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Test & MEASUREMENT WORLD

THE MAGAZINE FOR QUALITY IN ELECTRONICS

Ultrasound's war on prostate cancer

Engineers at Focus Surgery rely on a full arsenal of tests to validate a noninvasive alternative to surgery and radiation.

Page 24

Naren Sanghvi, co-founder and chief scientific officer of Focus Surgery.

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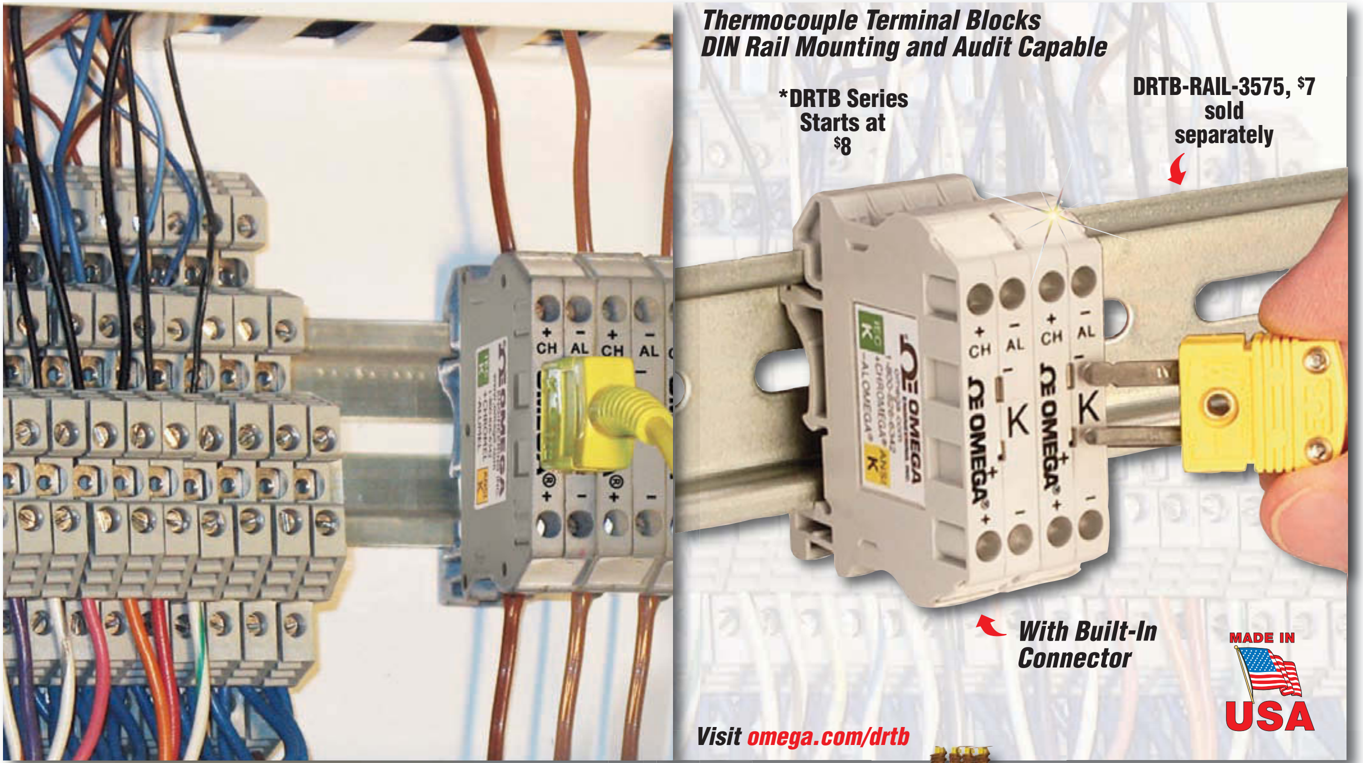

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VOL. 31 NO. 6

CONTENTS

COVER BY: BASS PHOTO CO.

Test voices / Page 11

DEPARTMENTS

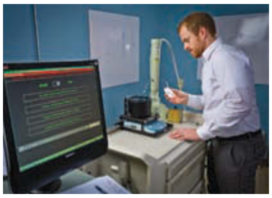
FEATURES

TEST IDEAS

22 **Modular system simulates a space payload**
Simulating the payload lets engineers test I/O interfaces.
By Mathew Maher, Surrey Satellite Technology Ltd., Surrey, UK

MEDICAL ELECTRONICS TEST COVER STORY

24 **Ultrasound's war on prostate cancer**
Engineers at Focus Surgery rely on a full arsenal of tests to validate a noninvasive alternative to surgery and radiation.
By Lawrence D. Maloney, Contributing Editor



SEMICONDUCTOR TEST

32 **PXI boosts IC test**
Digital-isolation and broadcast-receiver device-test examples illustrate the capabilities of a PXI-based semiconductor test system.
By W.R. Bottoms, S.K. Sathish, T. Velmurugan, and D. Rajakumar, 3MTS; and Michael Dewey, Geotest—Marvin Test Systems.

DESIGN TEST

36 **Debugging low-power designs**
A logic analyzer and an oscilloscope can help you debug embedded systems designed with energy-management techniques.
By Gina Bonini, Tektronix

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Introducing the NTAF spec

As networks become more complex, the testing of network equipment requires multiple tools. Automation is frequently employed as a strategy to orchestrate the diverse test environment, but to date there have been no standards for tools to work together in a coordinated solution. The NTAF (Network Test Automation Forum) has addressed this need by defining a specification for how test tools communicate.

An archived Webcast on the *Test & Measurement World* Website introduces the NTAF, explains the organization's recently ratified specification, and walks you through an example application. Senior technical editor Martin Rowe served as moderator of the presentation.

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T&MW blogs

Taking the Measure

Rick Nelson, Editorial Director

- Analog guru Jim Williams dies
- IMS2011: Test can address engineers' nightmare

Rowe's and Columns

Martin Rowe, Senior Technical Editor

- The Internet was tested
- Network test spec approved
- Help Luis play back waveforms

Testing the Limits

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- Communications testing in a power line environment
- 40 and 100 Gigabit Ethernet (802.3ba) testing challenges
- EEEk!: Energy Efficient Ethernet testing challenges
- Ethernet: not so easy

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Evolutions

Richard Quinnell, Contributing Technical Editor

- Signaling overload stalks LTE
- Pandora's privacy puzzle
- LTE to save planet

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RICK NELSON
EDITORIAL DIRECTOR

Prospects for RF MEMS

Are RF MEMS devices commercially viable, or will they become so soon? That question was addressed at a 2011 International Microwave Symposium panel discussion titled "Commercial viability of RF MEMS—a reality or a dream?"

The short answer is yes, RF MEMS devices are commercially viable. Back in 2009, Omron was already selling its 2SMES-01 10-GHz RF MEMS switches into high-throughput ATE applications. Of course, even then, RF MEMS switches faced competition from other devices including Peregrine Semiconductor's UltraCMOS SOS (silicon on sapphire) devices.

The consensus was that MEMS makers will rise to the challenges.

Better questions—and in fact the ones addressed during the panel discussion—include, "Are RF MEMS a reality for my application, and if so, do they represent the best choice?"

For Agilent Technologies, RF MEMS devices with the performance demanded by the company's instrument divisions are not yet reality. Robert Shimon, a manager and principal engineer at Agilent's Santa Rosa, CA, facility, said Agilent would gladly purchase commercially available RF MEMS if they met performance specs, such as bandwidths to 67 GHz, 100-million-cycle reliability, and 10-dBm power-handling capability. He said the question regarding devices meeting such performance specs is when, not if, and he predicted they will be populating Agilent boxes within five years.

Tomonori Seki, a senior manager and principal engineer at Omron, took the stage to tout Omron's success with its 2SMES-01 devices, which he said offer insertion loss of less than 1 dB at 10 GHz. He said a more compact version for mobile applications is under development and will sample this summer.

Dylan Kelly, a manager and principal engineer at Peregrine, said his firm's SOS devices are already in mobile applications; for handsets, he said, SOS is no longer an exotic technology but is now mainstream. He said that if you need low loss and high frequencies (beyond 10 GHz), then you want to consider RF MEMS. Otherwise, he said, SOS will meet your application needs.

Weighing in on the side of MEMS were Art Morris, CTO of WiSpry, and Dennis Yost, president and CEO of Cavendish Kinetics. Morris said WiSpry has delivered thousands of tunable RF MEMS components and is ready to ramp up volumes in 2012. Yost said his company will also see volume shipments of its tunable-antenna RF MEMS devices in 2012 and will pursue additional applications in 2013.

Of course, just because a MEMS device meets your specs does not mean that the device is the best option for your application. As Julio Costa, director of technology development at RFMD put it, handset companies, for example, are not waiting for RF MEMS. They will continue to make handsets regardless. The issue MEMS makers must address, he said, is whether they can provide a viable solution that offers a performance improvement over what customers can currently get.

The consensus of the panel, organized by Gabriel M. Rebeiz of the University of California at San Diego and N. Scott Barker of the University of Virginia, was that MEMS makers will rise to the challenges. Concluded Yost of Cavendish Kinetics, "Five years from now, no one will be arguing about RF MEMS." T&MW

> > > *POST YOUR COMMENTS AT WWW.TMWORLD.COM/BLOG.*

Measurements demonstrate transceiver quality

Ousama Hage is a system I/O specialist at Xilinx in Ottawa, ON. He provides technical support to engineers who design systems with FPGAs that include from four to 96 serial links with data rates from 100 Mbps to 28 Gbps. Hage demonstrates the serial links to customers by making signal-integrity measurements, which he also uses to help engineers debug systems. Senior technical editor Martin Rowe spoke to Hage by telephone.

DANIEL GUIDERA

Q: What do you show customers in a demonstration?
A: Demonstrations let engineers see the performance of a Xilinx MGT (Multi-Gigabit Transceiver) through views of a transmitted eye diagram at a given data rate. Customers look at Dj (deterministic jitter), Rj (random jitter), amplitude, rise time, fall time, and jitter decomposition. I use an Agilent Technologies DCA-X oscilloscope to run PRBS7 or PRBS31 data patterns.

Many customers have signal-integrity teams, particularly for systems that use high-density backplanes with several high-speed serial transmission lines. For those customers, an evaluation may take several weeks to perform. Customers typically use evaluation boards to integrate an MGT into their system. They introduce noise and crosstalk and evaluate transmission performance on each channel. A channel's trace length ranges from 3 in. to over 20 in. with various types of high-density connectors.

Q: Do you bring test equipment to customers or do you rely on customer's test equipment?
A: At first, I may bring a DCA-X with a clock-recovery module to a customer site. The oscilloscope lets me demonstrate the transmit eye's performance. For longer evaluations with a customer who has a signal-integrity team, I use both my equipment and the customer's.

I used to bring a sampling oscilloscope to the customer site every time. Now, I use FlexDCA software in my lab to capture and record the performance of a transmitter at a particular data rate. I then bring the data to the customer and play it on my computer. Some engineers, though, still prefer an oscilloscope and an evaluation board, so I may bring them. Over time, I'll be less likely to carry an oscilloscope.

Q: How do you compensate for losses in measurements?
A: At speeds of 10 Gbps and higher, a transmission line from the FPGA to the SMA connector degrades the signal. Customers might perceive that as degraded performance of the MGT. Fortunately, I can compensate for channel losses by de-embedding the channel effects from the observed results. To show the performance at any FPGA pin, I de-embed the loss introduced by the channel. Many customers have S-parameters of their transmission channel. I can plug the S-parameter into FlexDCA software to then embed the effects of their channel. In this manner, they can see what the transmitted eye would look like at the output of their channel.

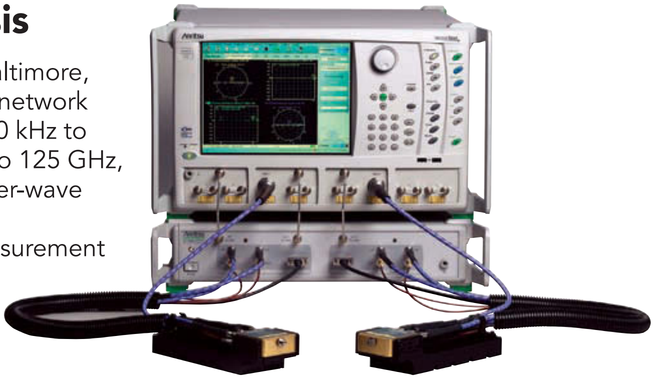
Q: What issues arise with engineers who use MGTs?
A: Customers run into issues such as power-supply ripple, PCB (printed-circuit board) material loss, and PCB layout. They need to avoid crosstalk, which often appears in connector via fields between two PCBs.

To guide designers, I generally rely on the customer's equipment for signal-integrity measurements. Most customers have high-speed oscilloscopes and clock sources. Some use TDRs (time-domain reflectometers) or VNAs (vector network analyzers) to measure channel loss and crosstalk. They use oscilloscopes to investigate analog power-supply rails, eye amplitude, and jitter. T&MW

This interview continues in the online version of this article, www.tmworld.com/2011_07.

Every other month, we interview an electronics engineer who has test, measurement, or inspection responsibilities. To participate in a future column, contact Martin Rowe at martin.rowe@ubm.com. To read past Test Voices columns, go to www.tmworld.com/testvoices.

Anritsu enhances vector network analysis



At the 2011 International Microwave Symposium (June 5–10, Baltimore, MD), Anritsu introduced the ME7838A broadband VNA (vector network analyzer) system, which provides single-sweep coverage from 70 kHz to 110 GHz. The total operating range of the ME7838A is 40 kHz to 125 GHz, which the system covers without requiring large, heavy millimeter-wave modules and coax combiners.

Bob Buxton, marketing manager for Anritsu's microwave measurement division, demonstrated the system at the symposium, using it in conjunction with a Cascade Microtech probe station for making on-wafer microwave measurements. He pointed out that the new design, which eliminates the need for external waveguides, minimizes the distance between device under test and measurement system to enhance accuracy. With the ME7838A design, millimeter-wave modules can be mounted close to or directly on the wafer prober. This advantage, as well as the fact that the ME7838A transitions at 54 GHz, gives the broadband VNA wide dynamic range of 107 dB at 110 GHz and 92 dB at 125 GHz.

The ME7838A targets applications including emerging 60-GHz wireless personal area networks, 40-Gbps and higher optical networks, 77- and 94-GHz automotive radar, digital radio links, 94-GHz imaging millimeter-wave radar, and Ka-band satellite communications. It can also conduct signal-integrity measurements on emerging high-speed designs, such as those incorporating 28-Gbps serializer/deserializer transceivers used on servers, routers, and other networking, computing, and storage products. Buxton pointed out that the system's use of smaller, lighter RF and millimeter-wave modules reduces the need for bulky positioners that add expense and can take up considerable lab space when the system is used on the bench. www.anritsu.com.

A2LA attains IAF MLA signatory status

The A2LA (American Association for Laboratory Accreditation) reports that it has been accepted as a member of the IAF MLA (International Accreditation Forum Multilateral Recognition Arrangement) for ISO/IEC Guide 65 Product Certification. The objective of the MLA is to cover all accreditation bodies in all countries in the world, thus eliminating the need for suppliers to be certified in each country where they sell their products or services.

In March 2010, A2LA was peer evaluated by the regional group, the IAAC (Inter-American Accreditation Cooperation), to expand its scope of recognition to include accreditation of product-certification bodies. In August 2010, the IAAC announced that A2LA had become a signatory to the IAAC MLA for product-certification bodies. Recently, IAAC was accepted by the IAF as a regional group for the IAF MLA to include product certification, which resulted in A2LA achieving the IAF MLA signatory status.

The requirements for a product-certification-body assessment are stated in ISO/IEC Guide 65, and they ensure users that an accredited body is competent and impartial. The A2LA accredits product-certification bodies that issue certificates attesting that an organization's quality-management system and its competence to certify products comply with a specified standard. www.a2la.org.

Editors' CHOICE

Agilent debuts peak power analyzer

Targeting the design, test, and validation of devices including power amplifiers, transceivers, and satellite payloads, Agilent Technologies' Model 8990B peak-power analyzer comes equipped with a 15-in. XGA color touch screen that can simultaneously display two RF channels and two analog channels. Complementing the 8990B are the new N1923A and N1924A wideband power sensors, which cover a frequency range of 50 MHz to 18 GHz and 50 MHz to 40 GHz, respectively. When combined with either sensor, the 8990B peak-power analyzer achieves a 5-ns rise time/fall time, making it suitable for RF pulse measurement and analysis in the military/aerospace and wireless industries.

The 8990B offers a sampling rate of 100 Msamples/s and comes with 15 predefined pulse-parameter measurement functions, including rise time, pulse droop, pulse width, and time delay. Users can execute the functions automatically in two steps via the touch screen. The LXI Class C instrument is available with an optional USB interface and an optional, removable hard drive.

Base prices: 8990B—$28,500; N1923A—$5000; N1924A—$5500. *Agilent Technologies, www.agilent.com.*

CALENDAR

International Symposium on Electromagnetic Compatibility, August 14–19, Long Beach, CA. *IEEE, www.emc2011.org.*

Autotestcon, September 12–15, Baltimore, MD. *IEEE, www.autotestcon.org.*

International Test Conference, September 18–23, Anaheim, CA. *IEEE, www.itctestweek.org.*

Productronica, November 15–18, Munich, Germany. *Messe München, www.productronica.com.*

To learn about other conferences, courses, and calls for papers, visit www.tmworld.com/events.

Editors' CHOICE

Audio tester adds Bluetooth

Cellphones use Bluetooth to send digitized audio to and from headsets, landline phones, and computers. To aid in the testing of such devices, Audio Precision has added a Bluetooth module to its APx500 line of audio testers. In addition to testing headsets and phones, the module lets the instrument test audio quality in Bluetooth dongles, Bluetooth adapters, computers, and automotive head units. It supports many popular audio codecs and it can make some 30 acoustic and electronic measurements including frequency response and harmonic distortion.

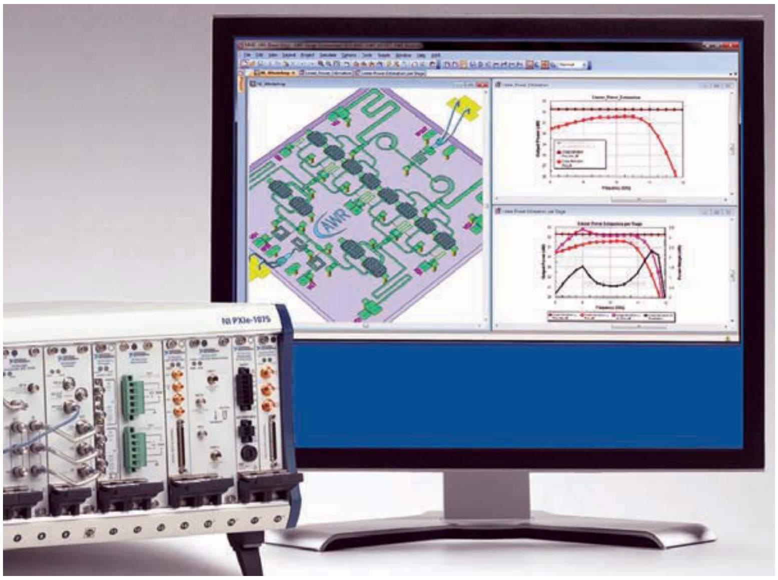
You can use the Bluetooth audio tester in combination with other tester modules in an APx audio analyzer to measure audio quality on complete audio systems. The Bluetooth option is compatible with the APx520, APx521, APx525, and APx585 models.

Under software control, the Bluetooth module can open a connection, ring a device, transmit audio, and receive audio. It can switch between several Bluetooth profiles and audio codecs. You can use the supplied software or write your own using LabView or Microsoft .NET.

Price: $4500. *Audio Precision, www.ap.com/bluetooth.*

Instruments and software address RF design and test

> > > International Microwave Symposium, June 5–10, Baltimore, MD, www.ims2011.org.



With the acquisition of AWR, National Instruments has added AWR's Microwave Office and Visual System Simulator to its LabView software and PXI-based RF testing hardware platform.

Courtesy of National Instruments.

National Instruments emphasized the benefits of close integration between design and test in the microwave application area by highlighting its recent acquisition of **AWR.** Together, the companies offer core software brands including NI LabView and AWR's Microwave Office and Visual System Simulator. The software offerings complement NI's PXI-based hardware platform for RF test, which NI augmented with its recent acquisition of **Phase Matrix.**

In other software news, **CST** (Computer Simulation Technology) announced the release of new high-performance-computing options as well as an Eigenmode solver for CST Microwave Studio 2011. The new release augments GPU (graphics processing unit) support and MPI (message passing interface)-based parallelization. The new Eigenmode solver helps determine parameters such as resonance frequencies and Q-values for resonant structures.

Agilent Technologies featured a variety of hardware and software products. It debuted the Model 8990B peak-power analyzer as well as five new PNA microwave VNA (vector network analyzer) models operating up to 67 GHz. Agilent also announced the release of Electromagnetic Professional 2011.07, a modeling and simulation platform that creates 3-D models and analyzes the electrical performance of packages, connectors, antennas, and other RF components. Agilent also highlighted a number of products it had introduced earlier this year, including VNAs and options as well as a line of instruments and software tools that address the evaluation of advanced radar and electronic-warfare systems.

NMDG released a new version of its ZVxPlus nonlinear extension kits for Rohde & Schwarz ZVA and ZVT VNAs. The new hardware/software kits extend coverage to 24 GHz. The company also said its ICE software platform now supports **Focus Microwaves'** MPIV modular pulsed IV system and Rohde & Schwarz's RTO oscilloscopes.

For its part, **Rohde & Schwarz** highlighted its new R&S ZNB and R&S ZNC VNAs, which feature a dynamic range up to 140 dB and a sweep time as low as 4 ms for 401 points. The ZNC covers 9 kHz to 3 GHz; the ZNB covers 9 kHz to 4.5 GHz or 8.5 GHz.

Anritsu introduced the ME7838A broadband VNA system. It provides single-sweep coverage from 70 kHz to 110 GHz without requiring large, heavy millimeter-wave modules and coax combiners. In addition, Anritsu announced that VNA frequency extension modules from **Virginia Diodes** will allow the Anritsu VectorStar VNAs to provide measurement analysis from 70 kHz to 750 GHz.

Complementing other LTE news at IMS2011, **Aeroflex** announced two new options for its 7100 LTE digital radio test set. The options support testing of 3G WCDMA/HSPA and GSM/GPRS as well as the data-call handover between LTE and HSPA. Aeroflex also said it has added support for popular avionics waveforms to its S-Series signal generator family. The new option supports avionics authorities (civil or military), airfields, airframe manufacturers, aircraft systems manufacturers, and military subcontractors who use avionics-specific signal generators to test important navigation functions.

W.L. Gore & Associates highlighted a rugged 18-GHz cable assembly that the company has added to its Gore PhaseFlex microwave/RF test assemblies line. This rugged cable assembly is specifically engineered for high-throughput production-test applications in the wireless infrastructure market.

Crystek Crystals debuted a low-phase-noise oscillator, a VCSO, and high- and low-pass filters. Its new HCMOS oscillator provides a −165 dBc/Hz noise floor and can serve in synthetic instrumentation based on VXI and PXI architectures. T&MW

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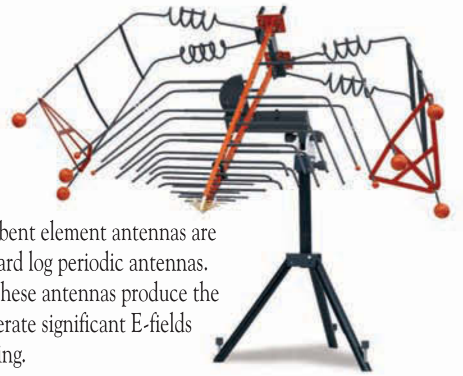

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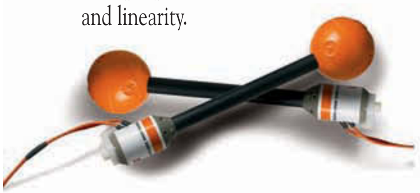

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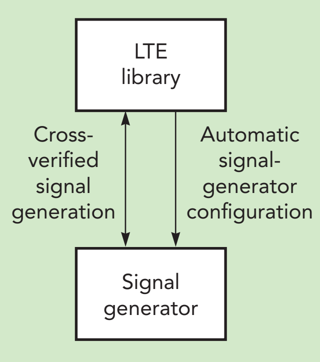
EDA and test companies team up on LTE

LTE is gaining considerable attention from design and test firms, with the most recent news coming from Rohde & Schwarz and Synopsys, which have announced a collaborative effort to accelerate the design and verification of LTE and LTE-Advanced wireless systems. That news complements recent LTE-related announcements from companies including Aeroflex, Agilent Technologies, Anritsu, and ETS Lindgren, as I reported on this page in May.

In the latest news, Synopsys is contributing its algorithm design and verification tools, including standards-compliant reference libraries. Rohde & Schwarz is contributing its signal generators, against which the Synopsys' LTE and LTE-Advanced libraries have been verified to increase designer confidence in achieving standards compliance when evaluating prototypes and samples.

Through the collaboration, the companies will verify Synopsys' LTE library for its System Studio and SPW tools, including upcoming LTE-Advanced enhancements, against the Rohde & Schwarz SMU200A and SMBV100A signal generators, which in turn will be able to automatically derive their configuration from the Synopsys simulation setup. Since typical configurations consist of more than 100 parameters, this integration reduces the time it takes to achieve a correct setup. The integration also reduces the risk of configuration inconsistencies that can result in losing days of system-integration time in the lab.



Rohde & Schwarz signal generators can be cross verified against the Synopsys LTE library, which in turn will support automatic configuration of the signal generators.

According to Markus Willems, senior product marketing manager for system-level solutions at Synopsys, and Simon Ache, product manager for signal generators and power meters at Rohde & Schwarz, Rohde & Schwarz and Synopsys found they were talking to many of the same companies but to different teams within those companies when marketing LTE-related offerings. While Synopsys was addressing concept engineers and algorithm designers, Rohde & Schwarz was addressing manufacturing engineers and chipset developers working with real silicon. The two companies realized they could collaborate on assisting both the algorithm designers and the chipset developers.

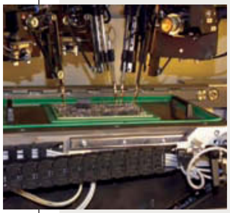
By making it possible for an LTE library to be validated against a signal generator, they said, the two companies are enabling I/Q signal equivalence for both algorithm designers and chipset developers. The use of a bit-equivalent I/Q signal throughout all phases of the design process from concept to final hardware test facilitates comparison and cross analysis throughout the process and increases confidence in standards compliance. In addition, the use of bit-equivalent signals simplifies debug should an inconsistency occur between simulation and hardware test.

From an instrument perspective, the SPW/System Studio automatic configuration capability reduces test-equipment setup time while avoiding wasted system-integration time because of configuration errors. It also ensures consistency of signal generation for both simulation and test, and it supports the reuse of regression scripts from simulation setup during the integration testing phase. T&MW

Goepel and SPEA team up on boundary scan

Goepel Electronic and SPEA have developed a boundary-scan option for the SPEA 4060 flying-prober test system. Within the integration, an automatic test-program-generation process combines in-circuit and boundary-scan test. Goepel provides integration packages that contain a controller for USB, LAN, and cabled PCI Express; a TAP transceiver with differential signal transmission; and TIC02/SR TAP interface card modules to be installed on the flying-probe shuttle. www.goepel.com; www.spea.com.

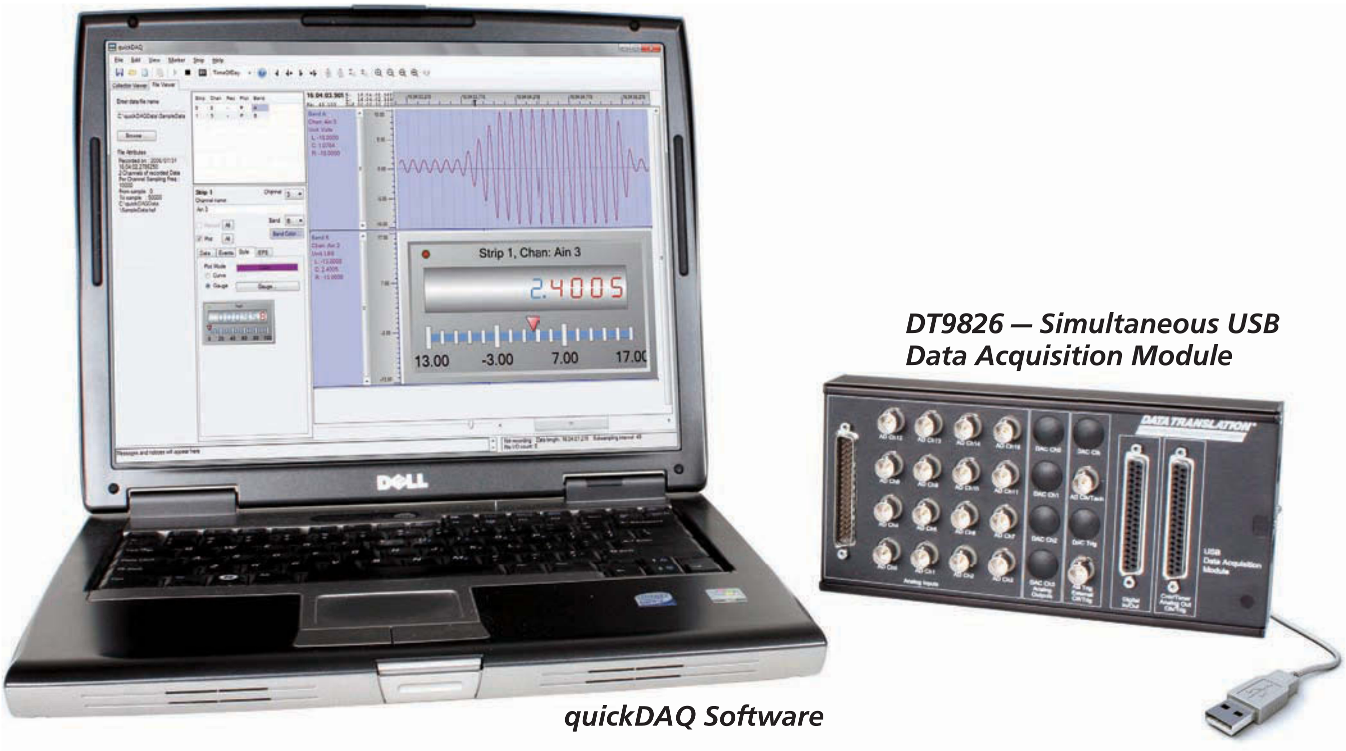
Boosting flying-prober throughput



Digitaltest reports it was able to augment a Condor flying-probe system that its customer EKM Elektronik had bought in 2003. A Digitaltest engineer designed a 90-pin vacuum fixture for EKM's Condor, enabling EKM to increase its board-test throughput from 30 boards to 70 boards in 8 hr. Digitaltest says the Condor permits functional tests using up to 1012 fixed probes through bottom-side access of a board. www.digitaltest.net; www.ekm-elektronik.de.

Test house chooses InCarrier

Multitest has received an order for InCarrier test equipment from a test house in Asia. The customer chose the InCarrier loader/unloader, an InStrip handler, and an InMEMS module for accelerometer MEMS test. InCarrier offers an alternative to standard singulated package test. www.multitest.com.



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USB Data Acquisition Module

ANN R. THRYFT
CONTRIBUTING TECHNICAL EDITOR
athryft@earthlink.net

IC package inspection gets complicated

Several trends in IC packaging, including changes in sizes and construction, are combining to make the inspection of packaged chips more complicated, difficult, and time-consuming. IDMs (integrated device manufacturers) and their subcontractors must inspect a wider range of package sizes and thicknesses, perform more substrate inspection for some package types, boost inspection accuracy, and increase the amount and accuracy of metrology.

Tools for inspecting packaged ICs, such as KLA-Tencor's CI-T620, must handle a wider range of package types and sizes, while increasing accuracy and throughput and making changeovers faster and easier. Courtesy of KLA-Tencor.

The sizes of final packages are changing in two directions, said Pieter Vandewalle, senior director of marketing for KLA-Tencor's ICOS Division. "There's a trend toward larger packages for high-end applications, and another toward smaller, thinner, higher-performance packages, mostly for mobile applications," he said. "Tools must now accommodate sizes from 2.5 mm x 2.5 mm to 66 mm x 66 mm." As packages get thinner, it's becoming more important to inspect warpage and cracks that may result from handling or testing them.

High-end package interiors are becoming more complex, requiring more inspection, said Vandewalle. Inside a typical package, dies are bonded to the substrate with wire bonding. The trend is to place more dies in a single package. In lower-performance packages, the dies are attached to the substrate via wire bonding.

"In higher-performance packages there's a shift to flip-chip attachment methods," he said. "A flip-chip package contains multiple dies and even multiple packages, so the final package and the substrate must be inspected. In addition, metrology is required for the bumps on both the die and the substrate."

CPUs and graphics processing units using this package type typically require 100% inspection of the substrate before the dies are mounted on it. The substrate's bump area consists of up to 10,000 bumps or more, and those must be measured with an accuracy of less than 1 micron at a rate of 1000 to 4000 substrate units per hour, he said.

Another complex package type that's becoming more common in logic and memory chips is package-on-package, said Vandewalle. Here, packaged ICs are stacked on top of each other using TMVs (through-mold vias), so the top side also has to be inspected using 3-D techniques. Other new technologies that increase inspection requirements include pre-mounted passives that require 2-D and 3-D techniques, TSVs (through-silicon vias) that must be inspected before molding, and dies embedded in the substrate.

To handle these IC packages, KLA-Tencor has combined the capabilities from several of its automated component inspection systems in the ICOS CI-T620, said Vandewalle. Its cost of ownership is lower and it is more user-friendly than previous generations of tools, he said, while the accuracy of final package inspection has been increased down to 5 µm via 3-D metrology. Downtime is minimized by a faster package changeover aided by dual tapers and a throughput increase of 70 to 80% over previous models. The system is designed for all tape and reel packages. T&MW

10-Mpixel GigE camera in right-angle version

The new uEye UI-5490HE GigE camera from IDS is available in an optional 90° angled housing for maximum flexibility in tight spaces. The camera's CMOS sensor outputs image data with up to 12 bits per channel depth, and it can capture 10-Mpixel images with square 1.67-µm pixels at 8 fps. The onboard FPGA is accompanied by 64 Mbytes of image memory. www.ids-imaging.com.

Inspection system targets advanced packages

Rudolph Technologies has introduced the NSX 320 automated macro inspection system for advanced packaging processes that use TSVs (through-silicon vias) to connect multiple die in a single package. The system also provides inspection capabilities for edge-trimming metrology, wafer alignment during bonding processes, and sawn wafers on film frames. www.rudolphtech.com.

Software adds inspection tools

Cognex's In-Sight Explorer 4.5 includes the Flexible Flaw Detection edge- and surface-inspection tool, the Bead Finder and Bead Tracker bead-width and bead-position tools, and the ReadIDMax tool. ReadIDMax reads up to 128 1-D bar codes or 2-D matrix codes at once, regardless of the code's position in the field of view, allowing In-Sight cameras to simultaneously read bar codes and conduct inspections. www.cognex.com.

FUNCTIONAL TEST

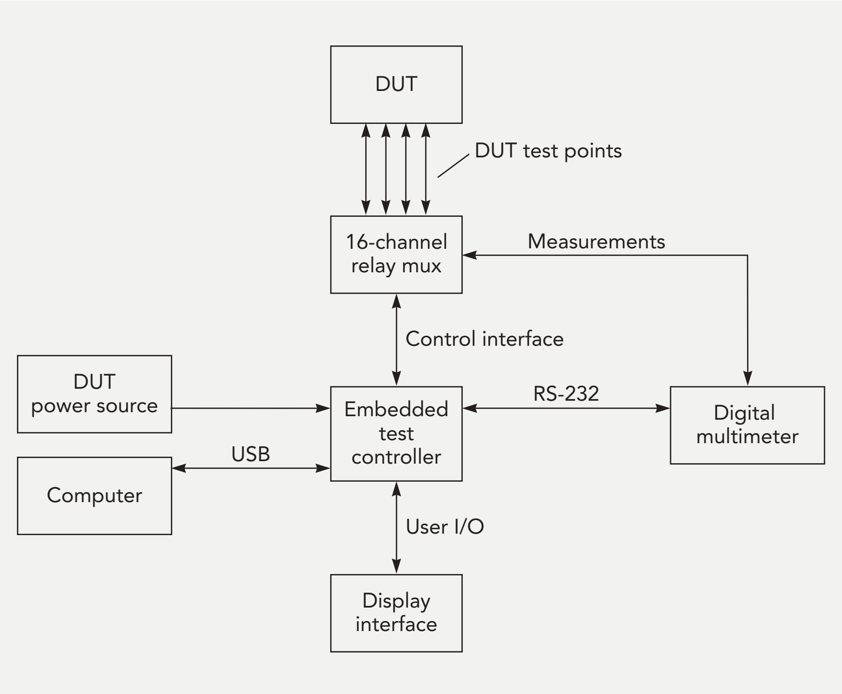
Build a tester around a microcontroller

While many engineers use PC-based test systems for functional test, sometimes such systems are too expensive or too impractical. Some test applications call for embedded intelligence to be built into a test fixture or stand-alone custom tester where test operators don't need a PC. When those circumstances arise, consider building a microcontroller-based tester.

A typical microcontroller has digital I/O ports, an ADC, and a serial port. You can use the digital I/O ports to control relays or other devices that can apply power and actuate a DUT (device under test) or provide status indication through LEDs. Digital I/O ports can also read a DUT's status. After the ADC digitizes analog signals, software can process the data, make decisions on DUT status, and take action. A serial port lets the tester communicate with external instruments such as multimeters that add more test capabilities.

You can learn how to build your own microcontroller-based functional tester by downloading "Build your own microcontroller-based functional tester" by Overton Claborne, president of Overton Instruments, from the online version of this article (www.tmworld.com/2011_07). In addition to describing how to design and construct the tester, Claborne also provides schematics, PCB (printed-circuit board) layouts, and source code that you can download.

Martin Rowe, Senior Technical Editor



A microcontroller-based embedded tester can connect to relays, power sources, instruments, and a host computer.

TEMPERATURE MEASUREMENT

Log amp linearizes thermistors

Thermistors make good choices as temperature sensors when you need fine resolution over a relatively small temperature span. Unfortunately, a thermistor's resistance-temperature curve has a nonlinear negative slope.

Engineers use a variety of techniques to linearize the curve. For example, researchers at the Department of Electrical Engineering at the Indian Institute of Technology Madras have developed a system that uses a logarithmic amplifier in front of an integrating ADC to digitize resistance and convert it to temperature. The researchers tested the circuit at temperatures from 0°C to 120°C. They published a paper describing their work in the May 2011 issue of *IEEE Transactions on Instrumentation and Measurement* (Ref. 1).

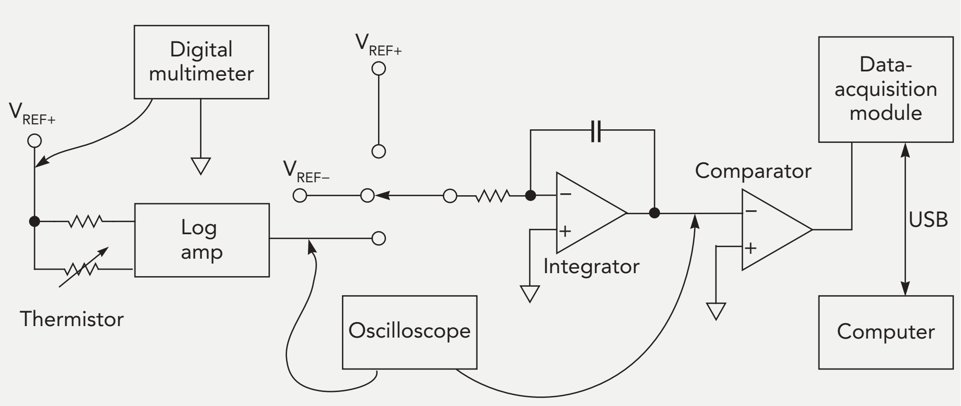
The system, which the researchers first simulated and then tested with real components and test equipment, consists of a voltage reference, a log amp, an integrator, a comparator, and a USB data-acquisition module. The **figure** shows a simplified schematic.

The integrator's capacitor charges from reference voltages for a fixed time. As the capacitor discharges, the data-acquisition module's internal counter/timer counts clock pulses. The data-acquisition unit's digital output represents temperature, which the module sends to a PC over a USB link. The PC need not linearize the digital output, nor does it need to convert from ADC counts to temperature.

The researchers used one of the data-acquisition module's digital I/O pins to read the comparator's output. The comparator output indicates when a conversion takes place. Other I/O pins control the switch, changing it among positive and negative reference voltages (V_{REF+}

and V_{REF-}) and the log amp's output voltage.

Performing error analysis, the researchers learned that several circuit component values affect the measurement error. For example, the voltage reference plays a key role in the system's accuracy and stability. Offset voltages in the amplifiers also play a key role in limiting accuracy. The researchers note that "Variation of V_{LOG} [the log amp's output] by as little as 5 mV is sufficient to cause the measured temperature to be in error by more than 0.5°C."



A log amplifier and integrator form a linearizing ADC for a thermistor. The data-acquisition module includes a timer/counter and digital I/O.

A 6.5-digit multimeter monitored V_{REF+} and V_{REF-} during the tests. The oscilloscope provided a view of the log amp's output voltage and the integrator's output waveforms, which provided the researchers with confidence in their design. In the future, IC manufacturers could integrate the circuit's components into a single IC or into a specialized ADC for measuring temperature with a thermistor.

Martin Rowe, Senior Technical Editor

REFERENCE

1. Mohan, N. Madhu, et al., "Linearizing Dual-Slope Digital Converter Suitable for a Thermistor," *IEEE Transactions on Instrumentation and Measurement,* May 2011. www.ieee.org. (The authors have also posted the paper on their own Website: bit.ly/li1mg8.)

Modular system simulates a space payload

Simulating the payload lets engineers test I/O interfaces.

By Mathew Maher, Surrey Satellite Technology Ltd., Surrey, UK

At SSTL, we recently designed satellite payloads for launch on partner-system satellite platforms. To minimize development time, we developed a payload simulator that lets us test the interfaces between the platform and its payload.

The simulator simulates more than 500 I/O channels that cover several electrical standards and formats. It uses closed-loop control for its signals because it must reproduce dynamic payload signals based on inputs. Most of the hardware is standard off-the-shelf test equipment that resides in a 19-in. rack. **Figure 1** shows the system diagram.

The host PC is a workstation-grade computer with a quad-core Intel Xeon processor that runs Scientific Linux. It provides a stable and close-to-real-time platform to run the bespoke command-and-control application software. A hardware-based remote-access device routes all user control over Ethernet to a remote console that has a keyboard, mouse, and monitor.

A GPIB link connects several instruments to the workstation. A 1200-W power supply from TTi provides 50VDC to the integrated flight units. These flight units are used to provide functionality that is not cost-effective to simulate, such as RF communications. A TTi signal generator produces clock signals for the flight transmitters and receivers. Finally, two Agilent Technologies electronic loads add 15 channels of simulated current consumption. With those loads, the simulator can load the satellite power system in a way that represents the payload.

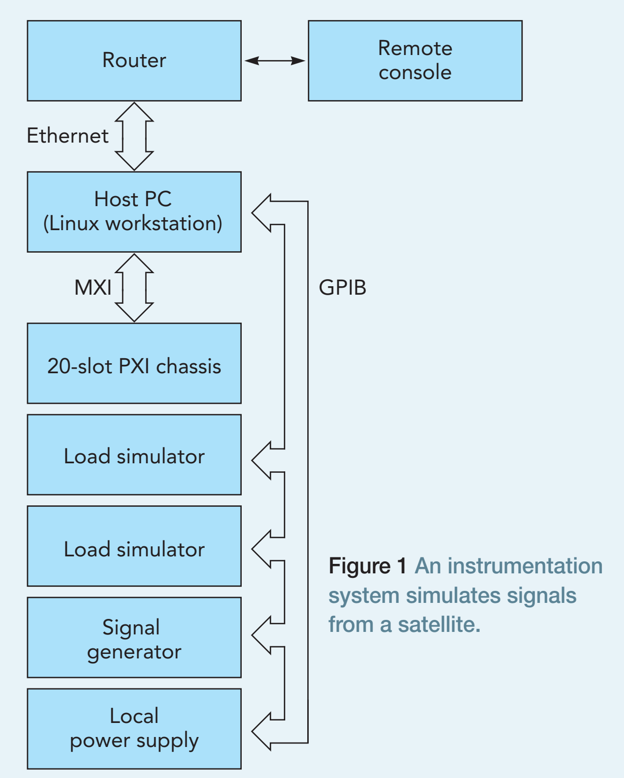


Figure 1 An instrumentation system simulates signals from a satellite.

An MXI interface connects the workstation to a Geotest 20-slot PXI chassis that houses most of the electrical interfaces (**Figure 2**). The chassis provides a second line of defense in the event of overtemperature or overvoltage failure. Should either condition occur, the software will perform a controlled shutdown and advise the operator. Any equipment failure can easily cost more than $1.5 million in flight equipment and can push development programs beyond planned launch dates.

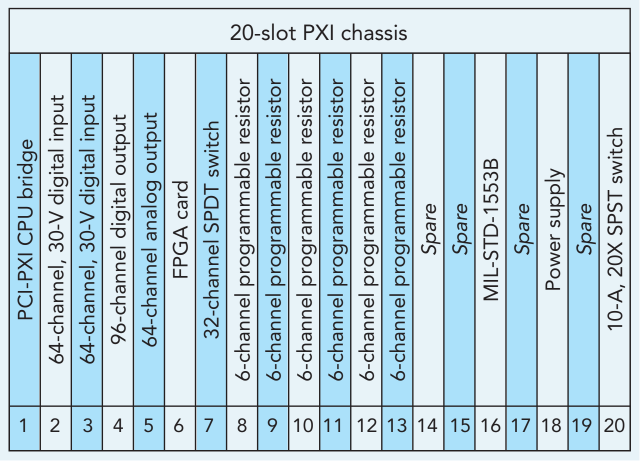
The PXI chassis also houses two National Instruments 64-channel, 30-V input cards that detect 28-V pulses. These cards provide both rising-edge and falling-edge detection, which means we can calculate pulse width. This software pulse-width detection gives us a quick way to measure software performance. In one software test, we ran the system on both Linux and Windows and attempted to measure pulse width. Running Windows, the system couldn't accurately measure pulses below 15 ms, whereas Linux consistently lets us measure pulses down to 1 ms.

We also use a National Instruments 96-channel digital-output card to provide basic TTL signaling, and we use a 64-channel analog-output card from Geotest to produce slow-update analog signals from 0V to 5V. The main satellite uses these analog signals to monitor slow-moving signals from the payload units.

Because space-standard interfaces often differ from commercial interfaces and protocols, we can't always purchase off-the-shelf items for testing. In this instance, we use a Geotest FPGA card to provide a specialist six-wire serial-interface protocol. This reprogrammable card lets us reuse VHDL code developed for the satellite payload directly on the simulator with little modification. Attached to the FPGA card are custom-made differential signaling adapters that provide the space-standard electrical format. These external adapters also provide a level of fault isolation between test equipment and the DUT (device under test).

A Pickering Interfaces 32-way switch simulates RF-switch-feedback contacts, and a 10-A switch card connects satellite power sources to the electronic-load channels. Six precision-programmable resistor cards provide 36 channels of thermistor simulation from –55°C to +90°C. Both switch and resistor cards use mechanical relays, which isolate the simulator from the platform.

A Pickering Interfaces isolated power-supply card gives the system three +5-V power supplies to the external dif-



20-slot PXI chassis																			
PCI-PXI CPU bridge	64-channel, 30-V digital input	64-channel, 30-V digital input	96-channel digital output	64-channel analog output	FPGA card	32-channel SPDT switch	6-channel programmable resistor	6-channel programmable resistor	6-channel programmable resistor	6-channel programmable resistor	6-channel programmable resistor	6-channel programmable resistor	*Spare*	*Spare*	MIL-STD-1553B	*Spare*	Power supply	*Spare*	10-A, 20X SPST switch
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

Figure 2 The system's PXI chassis contains analog-output modules, an FPGA module, and switch modules.

ferential signaling adapters used on the serial-communications channels. This card employs onboard DC-DC converters that isolate the internal PXI chassis power rails from the DUT. T&MW

Wide Band Clamp-on Current Monitor

Pearson Electronics is pleased to introduce a new line of Wide Band Clamp-on Current Monitors. The new design features a ½ inch or 1 inch aperture with a hinged type opening for easy operation. The new design incorporates Pearson's wide band frequency response in a demountable configuration for use on fixed conductors.

The model 411C, typical of the group, has a sensitivity of 0.1 V/A, a 3dB bandwidth from 25 Hz to 20 MHz, and a 5,000 amp peak current rating. Pulse rise times down to 20 nanoseconds can be viewed. Accuracy of 1%, or better, is obtainable across the mid-band.

Other models feature a 2.0 nanosecond rise time, or droop as low as 0.003% per microsecond.

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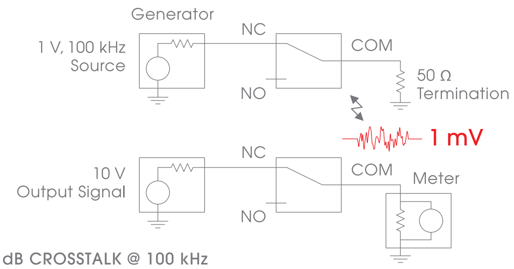

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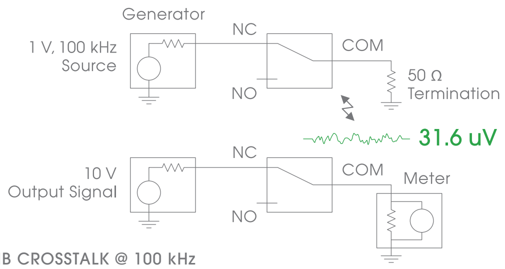

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Chief scientific officer Naren Sanghvi and the engineering team at Focus Surgery perform both hardware and software tests to verify the therapeutic and diagnostic benefits of the Sonablate 500 ultrasound system.

PHOTO BY BASS PHOTO CO

Ultrasound’s war on prostate cancer

Engineers at Focus Surgery rely on a full arsenal of tests to validate a noninvasive alternative to surgery and radiation.

BY LAWRENCE D. MALONEY, CONTRIBUTING EDITOR

INDIANAPOLIS, IN—This year, according to the American Cancer Society, nearly 220,000 men in the US will be diagnosed with prostate cancer, the second most common cancer affecting males after skin cancer. More than 32,000 will die of the disease.

Until recently, the choices for treating this disease, which affects one in every six males at some point in their lives, have typically involved either radiation or radical surgery to remove the entire prostate, a procedure that frequently leads to incontinence and impotence. Now, companies are developing alternative technologies, based on cryotherapy or ultrasound, which target only the cancerous area of the prostate and offer less of a threat to a patient’s future quality of life.

A leader in offering such new approaches is Focus Surgery, the Indianapolis-based unit of US HIFU, whose international arm is already marketing its Sonablate 500 ultrasound system in 33 countries, including Canada, Japan, and the UK. Currently, the system is undergoing clinical trails in the US, but hundreds of American men have already received treatment with the device at offshore medical facilities (see “Journey to market for the Sonablate 500 ultrasound system” in the online version of this article, www.tmworld.com/2011_07).

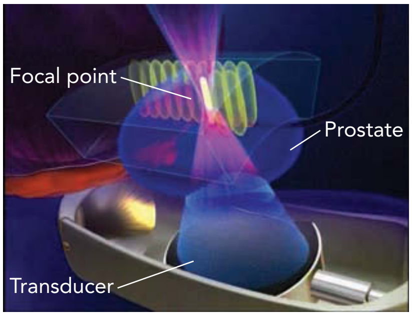

FIGURE 1. Containing both imaging and ablating elements, the Sonablate’s transducer alternates between high-energy power for ablation (3 s) and low-energy power for imaging (6 s). Courtesy of US HIFU.

With technology roots that go back to ultrasound pioneer Francis J. Fry’s research work at Indiana University Medical Center in the late ’80s and early ’90s, the Sonablate 500 offers a unique blend of imaging and ultrasound ablation techniques.

“We’ve improved the system continuously over the years,” said electrical engineer and Focus Surgery cofounder Naren Sanghvi, who developed with Fry an early ultrasound prototype device to treat benign prostatic hyperplasia. “We had to address such challenges as reducing treatment time, improving accuracy, and developing an effective water-cooling method to protect the rectal wall for the treatment of prostate cancer,” added Sanghvi, who is also the company’s chief scientific officer.

To validate the system’s many therapeutic and diagnostic benefits, Sanghvi and his engineering team employ test tools ranging from classic ultrasound-verification units and Schlieren beam-characterization techniques to software programs that create 3-D images that help them calculate the ideal shape and intensity of the ultrasound pulses.

Image-guided treatment

The current version of the Sonablate 500 consists of three main subsystems: a console unit containing a monitor, a keyboard, an RF amplifier, and electronics for ultrasound imaging, motion control, and I/O; a 60-cm probe containing positioning motors and actuators as well as the ultrasound transducers; and the Sonachill system for circulating degassed water at 16°C to 20°C to cool the transducer and the rectal wall during treatment.

What is especially notable about the Sonablate 500 is its piezoceramic transducer (**Figure 1**), which is situated at the very tip of the probe that the urologist places into the rectum after the patient has received anesthesia. The transducer design incorporates both an imaging element at the center core of the transducer and an ablation element in the outer area. In addition, the transducer is double-sided, so it provides a focal-length option of 3 cm or 4 cm. System software directs the transducer to move automatically and precisely to the target zone, based on the treatment plan developed by the physician after imaging the prostate prior to this outpatient operation.

During the procedure, the RF amplifier and associated electronics used for imaging, operating at 4 MHz, deliver a continuous ultrasound wave through the transducer to ablate cancerous tissue. Typical acoustic intensity is 1300 to 2200 W/cm^2 at the focal point. Total acoustic power is typically set at 24 and 37 W respectively for the 3- and 4-cm transducers. Each of the HIFU (high-intensity focused ultrasound) ablation shots creates a cigar-shaped lesion about 10 to 12 mm long, 3 mm wide, and 3 mm in diameter. Lesions overlap to create a continuous zone of ablation. The transducer alternates between high-energy power for ablation (3 s) and low-energy power for imaging (6 s).

What is especially distinctive about the system is that a physician can view the results of the procedure in real time in 2-D on the console monitor, and 3-D visualization is available as an option. To further enhance the treatment's effectiveness, Focus Surgery has added several features to the Sonablate system in recent years, noted Wohsing Chen, a PhD bioengineer who directs the company's R&D efforts. Among those advancements:

- The planned integration of a 6.5-MHz pulser-receiver for the imaging portion of treatment to achieve higher-resolution results.
- A TCM (tissue-change monitoring) feature that quantifies the extent of tissue ablation, based on spectrum analysis of the difference in RF pulse-echo signals before and after a HIFU ablation. A color overlay on the treatment-zone images shown on the console screen tells the physician if the tissue change was minor (green), moderate (yellow), or extensive (orange).
- The addition of a Doppler board to detect NVBs (neurovascular bundles). With this added capability, the transducer can detect areas within the prostate that house blood vessels so the physician can avoid ablation in those sectors.

"These changes are all the result of feedback that we have received from physicians and patients," said Chen. "So, we continue to move ahead on Sonablate 500 improvement projects, such as tissue-change monitoring. Temperature measurements are still the biggest challenge in ultrasound imaging devices, which is why we based our TCM method on detecting tissue change rather than absolute tissue temperature."

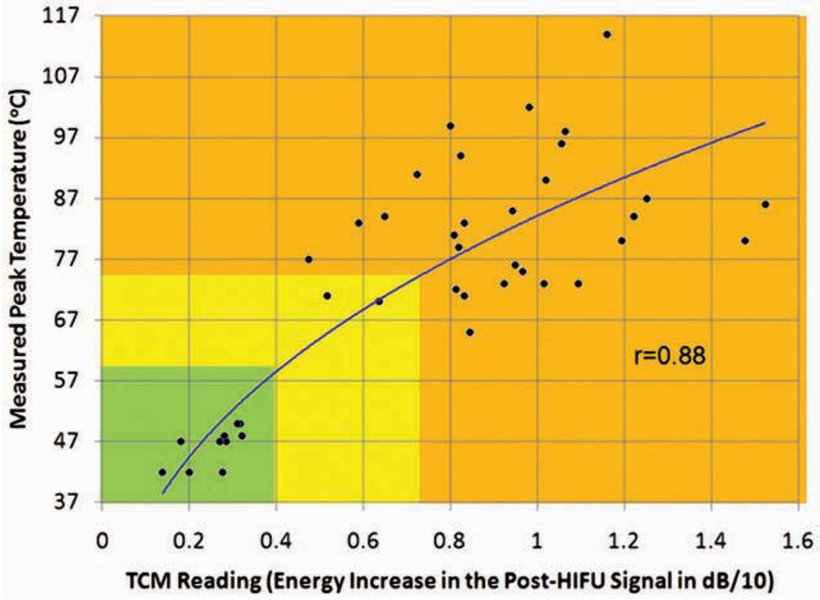

FIGURE 2. New features in the Sonablate include TCM (tissue-change monitoring), which quantifies the extent of tissue ablation, based on spectrum analysis of the difference in RF pulse-echo signals before and after a HIFU ablation. A color-code system on the console tells the physician if the tissue change was minor (green), moderate (yellow), or extensive (orange). Courtesy of US HIFU.

A matter of physics

The challenge of developing and improving the Sonablate requires a full arsenal of test tools, both hardware and software. One frequently used test bed is the verification unit, which is basically a small tank filled with degassed water. When equipped with a variety of test fixtures, the unit serves as a valuable tool for analyzing many aspects of the ultrasound delivery system, such as TCM, image verification, NVB detection, and beam alignment.

"Water not only mimics the condition within the human body, but it also offers excellent acoustic properties," explained Chen, "so you can get effective ultrasound penetration with no energy loss."

In early tests during the development of the TCM feature, engineers preheated a chicken breast to 30°C and submerged it in a fixed position in the tank. Using the HIFU probe and transducer, the team performed the normal HIFU treatment cycle of 3 s on and 6 s off in a succession of positions, gradually decreasing the TAP (total acoustic power) from 35 W to 5 W. Team members measured the temperature of the chicken breast with a thermometer and thermocouples they had placed in the sample before submerging it. Performing the same test multiple times, the team then calculated the relationship of temperature to increased energy, measured in decibels.

Researchers also validated this calculation when they treated prostate cancer patients with real-time thermometry. These tests helped determine the energy and temperature requirements needed to produce specific tissues changes, paving the way for the green-yellow-orange indicator on the console screen (**Figure 2**).

Similarly, to test the Doppler system's ability to locate blood vessels for NVB detection, the team stations a gel-like plastic "phantom," similar in consistency to a prostate, in the verification tank. A pulsative pump pushes a blood-like substance through tubes inserted in the periphery of the phantom to mimic

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blood flow. The Sonablate itself triggers the ultrasound pulses for imaging, with results shown on the console monitor.

Senior production engineer Maksim Kuznetsov also uses the verification unit to perform manufacturing tests on the Sonablate 500 at the Indianapolis site. One test involves placing an acrylic block in the water-filled tank and subjecting it to ablation shots of varying duration and intensity in prescribed locations, creating "lesions" of a specific size and shape.

"The test helps to verify the size and shape of the ultrasound beam," noted Kuznetsov. "The block is sent with the Sonablate unit when it is shipped, and the field engineer will perform the same test on a second block and compare lesions on the two blocks through a polarized film."

Also valuable to both manufacturing and field engineers is another test featuring a shell-like piece of acrylic with a curvature of 3.5 cm. Analyzing the path of lesions created by the transducer along the inner surface of the shell helps verify the accuracy of the ultrasound beam and the precision of the device's motion-control system. The distance between any two lesions should be no more than 1 mm.

To test the system's TAP, engineers use a different verification tank, this one with sides and bottom covered with sound-absorbing rubber. The team mounts a rubber-covered plate inside the tank and attaches the plate to a metal lever that runs up the side of the tank and links to an acoustic power meter on the outside. Ultrasound pulses from the transducer create pressure on the plate, and this pressure is transmitted to the power meter. Essentially a very sensitive scale, the power meter converts this pressure to watts of acoustic power. During a typical Sonablate procedure, the physician uses a software slide control to lower or increase acoustic power as needed. Currently, Focus Surgery is developing software to automate the TAP tests, which will be particularly beneficial as the company introduces more complex transducers, such as one that features an annular or 2-D phased array.

Testing key components

Much of the Sonablate's performance depends upon the design of the system's transducers and the beam profiles they create during treatment. Focus Surgery manufactures its own transducers, including a unit small enough to fit through a trocar for laparoscopic ultrasound ablation of soft tissue, such as during treatment for kidney cancer.

One valuable tool used in the design of the transducers, as well as in the characterization of the acoustic beam itself, is a Schlieren imaging system. Focus Surgery uses an OptiSon system from Onda. This system projects a fiber-optic beam of monochromatic light through a collimating lens and into a water tank, where

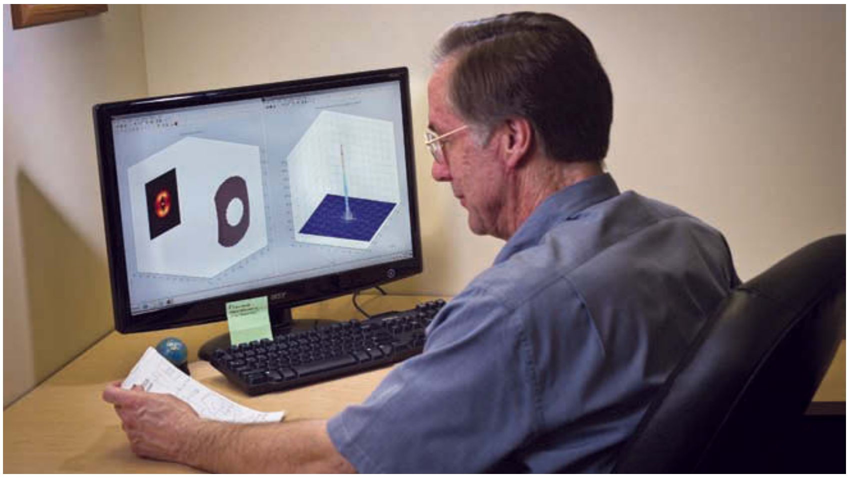
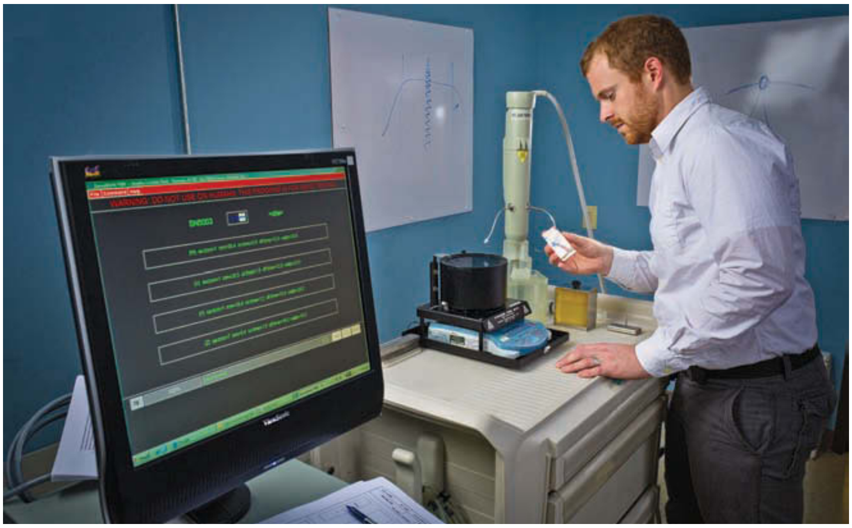


PHOTO BY BASS PHOTO CO

FIGURE 3. Senior software engineer Roy Carlson uses Focus Surgery's home-grown "bio-heat" simulation tool to estimate the shape of the ultrasound beam profile, the temperature distribution, and the size of lesions created by the ultrasound procedure.



Engineer Chris Cummings inspects an acrylic block that was ablated in a test using a water-filled verification unit.

PHOTO BY BASS PHOTO CO

an ultrasound transducer is submerged. A function generator and an RF amplifier drive the transducer, which fires a continuous wave of ultrasound perpendicular to the collimated beam. A focusing lens at the other end of the water tank directs the light onto a knife stop that blocks most of the light. The light that is refracted by the acoustic beam, however, misses the knife, and its beam profile is captured by a camera and shown on a monitor.

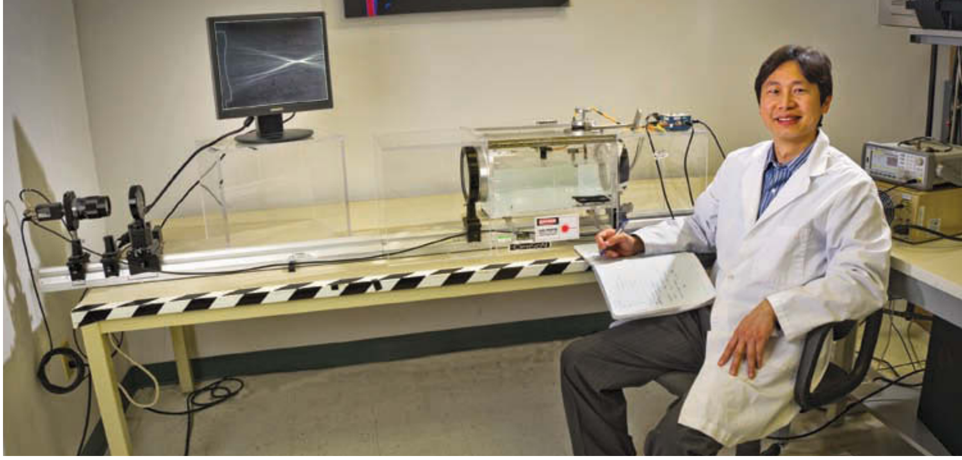
"It takes you about five minutes to do a Schlieren test, even with our double-sided transducers, versus several hours using a hydrophone, the traditional gold standard for measuring beam profiles," noted senior engineer Chris Cummings. "And the repeatability of your results is also very high. Plus, you get immediate visual feedback of the beam profile on a monitor, using a digital frame grabber to capture the image."

As a further QC step for transducers, Cummings also performs electroacoustic tests to determine the frequency response of the transducer's imaging element, a key factor in image resolution. In one test, a submerged transducer fires a short-duration pulse, generated by an Olympus pulser-receiver, onto a glass plate. The reflected response is analyzed on an Agilent Technologies oscilloscope. A broad bandwidth in an acoustic beam indicates a very short pulse and ensures the high resolution needed for imaging. Other electroacoustic tests measure the electrical impedance of the transducer element, as well as crosstalk.

Said Cummings: "These electroacoustic tests, along with the Schlieren and TAP tests, give you all that you need to characterize a transducer: beam shape, frequency, and power."

QC engineer Justin Fortner noted that emissions shielding was a key concern in the design of the console's custom enclosure and cabling. Focus Surgery outsources much of its IEC 60601-1 and -2 electrical safety and compliance testing to Underwriters Laboratories in Chicago, where the Sonablate is evaluated in UL's anechoic chambers. But the company also performs many of its own QC tests, both in manufacturing and in the field. Besides the tests already noted, other key tests include:

- RF amplifier test. In this procedure, the system's control system, featuring a National Instruments multifunction I/O card, varies the input voltage to the RF amplifier from 0 to 1 V, then measures the resulting RF sense voltage (0 to 4.8 V) and displays it on the Sonablate's console screen.
- Degassing and pump tests. The pump/chiller system includes an in-line vacuum pump and a filter to continuously remove gas from the water. During the ablation procedure, technicians use a calibrated pressure gauge to measure vacuum in mmHG (millimeters of mercury) and a CHEMets water-test kit to



Wohsing Chen, R&D director at Focus Surgery, works with a Schlieren imaging system, which serves as a valuable tool during transducer design.

PHOTO BY BASS PHOTO CO.

measure oxygen content. Pump tests also check for leaks and the stability of the latex sheath that covers the probe. Here, too, the NI multifunction board is used in operational tests.

Said Fortner: "Our field engineers not only perform many of the same tests that we do in manufacturing, but some of them are also qualified as sonographer technicians to monitor the equipment during operations."

The role of software tools

Focus Surgery engineers also make extensive use of software tools for design and test. Among the most important: SolidWorks software for creating a 3-D model of the probe housing and Matlab from The MathWorks for performing data analysis and prototyping.

R&D director Chen described the role Matlab plays in Focus Surgery's homegrown "bio-heat" simulation software, which the engineers use to estimate the shape of the ultrasound beam profile, the temperature distribution, and the size of thermal lesions, with results shown in 2-D and 3-D images (**Figure 3**). Based on heat-transfer equations, the software was written in C++, converted to MEX files by a complier, and then read into Matlab. With this tool, engineers can simulate any transducer geometry and can determine the amount of acoustic power needed for body tissues of varying density.

The Focus Surgery engineers also rely heavily on a special software package from Sonic Concepts to design their transducers. Called PiezoCAD, the software allows them to simulate electro-acoustic tests and determine such transducer parameters as transmit-receive efficiency. Along with OrCAD software from Cadence, the PiezoCAD package also aids in circuit design and PCB (printed-circuit-board) layout for the system's electronics.

The company's senior software engineers, Roy Carlson and Clint Weis, are involved in the design and test of virtually every aspect of the Sonablate system. In explaining how the system's 3-D imaging features work, Weis said, "The hardware basically images in 2-D, and we use software interpolation to construct volumetric 3-D images out of incoming data from 2-D image slices."

To verify those images and detect any distortions, Weis uses a verification unit to do a "rod phantom" test. Here, the transducer fires imaging pulse echoes at a submerged gel embedded with precisely positioned strings and bars of varying known thicknesses and material properties. The bars appear as different gray scales on the console screen.

Weis emphasized the close integration of all of the Sonablate's subsystems. "Everything in the ultrasound delivery system—the RF amplifier, the probe, and the transducers—is calibrated as a unit. If you need to replace an amplifier, all your probe calibrations are invalid."

A technology on the rise

The litany of tests the engineers perform on the Sonablate 500 also prove useful when Focus Surgery develops other ultrasound devices. The company has already received 510(k) approval from the FDA to market the Sonatherm 600i, which relies on the same essential Sonablate technology in a laparoscopic application to ablate cancerous tissue. The Sonatherm 600i combines image-capture and ablation capabilities in a probe whose outer diameter dimension is just 20 mm. The transducer performs continuous ablation, rather than using on-off cycles.

Among other devices, Focus Surgery has also developed for the US Army a robotically operated HIFU system for treating battlefield wounds. Operating at 2.2 MHz, the device can cauterize vessels from the skin surface to a depth of 70 mm. Still another research system, based on the Sonablate 500 platform, uses low-energy HIFU to build immunity against cancerous prostate cells by triggering the release of peptide heat-shock proteins in the blood.

Such applications are just a sampling of the many possible uses of ultrasound in medicine. "The growth of interest in therapeutic ultrasound in the last five to 10 years has been amazing," said US HIFU CEO Steve Puckett, Jr., who pointed to the rising influence of such organizations as the International Society for Therapeutic Ultrasound. "The core technology is extremely versatile, and more and more physicians and engineers are choosing ultrasound as a specialty."

For now, though, the big focus for US HIFU is getting the Sonablate 500 to market in the US. "That system is still our primary concern," said co-founder Sanghvi. "It has to be, because thousands are dying from prostate cancer. We see HIFU playing a significant role as the right balance between treatment and quality of life." T&MW

ON THE WEB

More than 30 countries have approved the Sonablate 500 for treatment of prostate cancer, but the system is still in clinical trials in the US. In "Journey to market for the Sonablate 500 ultrasound system" in the online version of this article, prominent urologists explain why they see the ultrasound procedure as a viable alternative to radiation and surgery: **www.tmworld.com/2011_07**

You can learn more about the technologies behind Focus Surgery's ultrasound systems by consulting technical papers on the company's Website: **www.focus-surgery.com/Publications.htm**

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National Instruments: PXIe-1075 User Manual, July 2008, 372437A-01 and 2008-9905-501-101-D Data Sheet

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PXI boosts IC test

Digital-isolation and broadcast-receiver device-test examples illustrate the capabilities of a PXI-based semiconductor test system.

BY W.R. BOTTOMS, S.K. SATHISH, T. VELMURUGAN, AND D. RAJAKUMAR, 3MTS; AND
MICHAEL DEWEY, GEOTEST—MARVIN TEST SYSTEMS.

The Model 3M20 combines PXI and proprietary instruments to minimize the cost of test for complex semiconductors.

Test is now a major portion of the total cost for many electronic products. In some cases, test costs even exceed fabrication costs, as a result of the fact that Moore's Law of scaling (Ref. 1) has driven down the cost of fabricating a transistor by more than a million times since it was first introduced about 45 years ago. The cost of testing a transistor, however, has not scaled at the same rate, and test is now threatening to be a limiting factor in the price-elastic growth of the electronics industry. The challenge for test engineers is to create test methods and systems that improve test quality while lowering test costs.

These challenges become more difficult as we approach the end of Moore's Law of scaling. The emergence of "More than Moore" functional diversification, which yields equivalent scaling (Ref. 2), further complicates test requirements and the economics of test. Today's SOC (system-on-a-chip) and SIP (system-in-a-package) architectures include many different circuit types in a single package (Ref. 3). Test resources must cover this ever-wider range of circuit types.

Logic and memory test capability alone is no longer sufficient as sensors, analog circuits, MEMS, and RF circuits become incorporated into a single package. These circuits are often stacked in 3-D structures, thereby increasing circuit density and improving power efficiency but limiting test access. And as device features have shrunk in size, transistors have increased in speed to the point where operating signal frequencies are reaching (and in some cases surpassing) the bandwidth of traditional probe cards and test sockets. Thus, manufacturers can no longer meet market demands for high-performance, low-power, low-cost devices with the "big iron" ATE (automated test equipment) systems that have tested most ICs over the past 40 years (see "PXI and the challenges of semiconductor test" in the online version of this article, www.tmworld.com/2011_07).

To keep pace with evolving technologies, some manufacturers are turning to PXI-based systems for semiconductor test. We recently built two such testers, one for a manufacturer of a digital-isolation device and another for a manufacturer of a digital broadcast receiver. These two examples demonstrate the effectiveness of a PXI-based alternative.

Digital-isolation device

In the first example, a manufacturer needed to test a serial-interface communication controller with a transformer interface that provides isolation for a point-to-point communication bus. The serial protocol uses an SPI-compatible interface, which is a four-wire bus with one clock and with latch-enable, data-in, and data-out signaling. The device requires high-voltage isolation up to 2500 V and supports data rates up to 20 MHz. It is used in smart-power-grid communications applications that require data acquisition and control signaling.

The manufacturer's incumbent tester had a number of limitations for the testing of this device: Its high-voltage power source required multiple external power supplies and was limited to a maximum of 1500 V; the cost of the high-voltage source and its external configuration resulted in an expensive applications load board; the tester could not address the required low leakage-current-measurement in picoamps; the tester and its tools didn't support characterization testing, which the customer performed using rack-and-stack instruments; and the capital and operating costs of the tester were far too high.

The manufacturer wanted a new, low-cost system that could perform a wide range of force and measure functions and serve in both characterization and production testing. 3MTS met this need by developing a system that uses PXI instruments to handle as many of the test requirements as possible (**Tables 1** and **2**). The 3MTS test platform leverages the VI (voltage/current) features of PXI instruments and also includes proprietary ATE instruments where PXI equivalents were not available.

Figure 1 shows the test head and the configuration of the PXI instruments. PXI instruments that do not require signal conditioning before they connect to the DUT (device under test) are wired directly through the test head to the SAB (socket-adapter board). The digital PXI instrument and the function generator pass through the wiring channels on the lower-left and lower-right sides of the test head and connect to the SAB as shown in **Figure 2.** Because this connection does not require slots in the upper card cage above the PXI card cage in the test head, we were able to increase the number of instruments available in the small test head (approximately 1 ft^3) of the system.

Digital broadcast receiver

The DUT in the second example is a digital broadcast receiver that has a built-in CMOS tuner and baseband chip. The high-performance device combines RF and digital logic with digital signal processing and also provides a high level of interference rejection. The device includes SPI, UART, I2S (inter-IC sound), SDIO, and serial flash control interfaces for seamless connectivity.

This long list of features complicates the testing of the device. The device manufacturer's existing tester was a traditional ATE system in a dual-site configuration. The manufacturer wanted to replace this system with a stable tester that would lower the overall cost of test, including the cost of multisite test. Test stability, cost of test, and cost for multisite testing are the big challenges for the existing system.

The 3MTS staff ported the manufacturer's tests to a 3M20 ATE system that incorporates PXI instrumentation, including the Geotest GX5295, a PXI-based 32-channel, 100-MHz DIO (dynamic I/O) instrument with a per-pin PMU (parametric measurement unit). **Table 3** contrasts the original tester with the PXI-based alternative. The new system reduces the total cost of test as a result of its much lower power requirements, reduced footprint, and reduced capital costs, which result from the use of reusable, industry-standard PXI instrumentation.

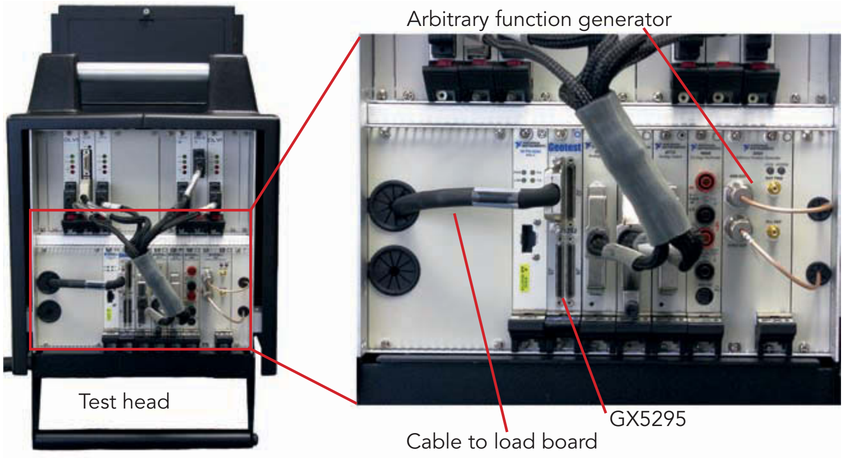

FIGURE 1. This PXI-enabled tester for a digital-isolation device incorporates PXI instrument slots, which accommodate a DIO board, data-converter boards, and an arbitrary waveform generator.

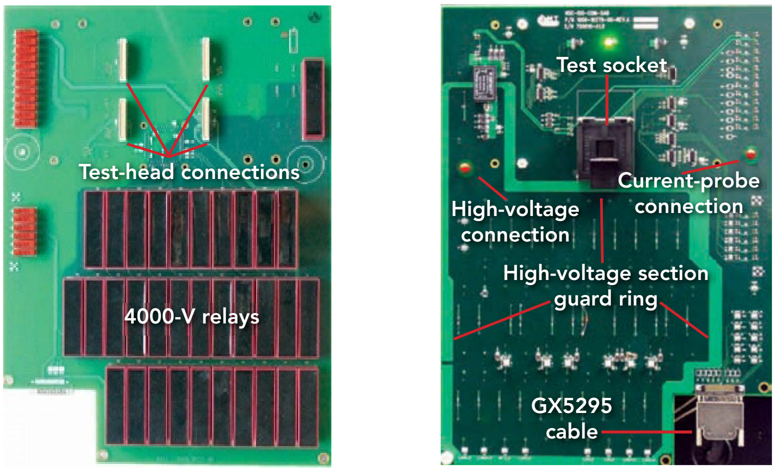

FIGURE 2. The socket-adapter board for the digital-isolation device connects resources from the test head via test-head connectors (left). The DIO PXI board connects to the DUT side of the adapter board (right).

The DUT side of the SAB (**Figure 3**) can accommodate dual-site testing. The RF instrumentation is located on the opposite side of the SAB, keeping the path length between the DUT and the RF instruments as short as possible for improved signal integrity. The GX5295 is routed through the test head directly to the SAB, providing both digital I/O capability and 32 PMU channels.

The new test system makes DC measurements, including continuity, leakage, and power measurements for various modes of operation. It also makes I_{DD} RF current measurements; gain and phase mismatch measurements as a function of modulation and amplification; structural tests, including, I_{DDQ}, BIST (built-in self-test), and scan; and system tests including SNR (signal-to-noise ratio), RSSI (received signal strength indication), and HDC (high-definition coding).

The GX5295 card tests the digital logic portion of the device, which has a data rate of 80 Mbps with pattern files of 60 million, 32-bit-wide vectors. The card is able to contend with the device's SPI protocol and SBL (surround-by-logic) formats, T-set variations, and dynamic changes of vector data, and it can decode digitized device ADC codes to real values. For testing the DUT's dynamic analog signals, the 3MTS engineers chose another Geotest module, the GX2472 high-speed differential digitizer, and they used Tessolve's TOTUS instrument-integration libraries to integrate an RF signal generator into the tester.

(continued)

Software tools

In order to force a stimulus and measure a response, a test system must have a means for generating and processing data. The same test system can be used during both characterization and production testing, but characterization tests generally require higher resolution so engineers can evaluate a device's electrical and signal-timing parameters. Traditional ATE systems often required reprogramming when moving from characterization to production testing. In contrast, a PXI-based tester that uses hardware-independent software does not require reprogramming; the system can perform both characterization and production tests. An added benefit of some PXI software programs is that they support automatic multisite testing, which again simplifies the move from characterization to production test.

Table 4 lists some of the standard software tools used for the two examples in this article. The online version of this article includes links to screen shots showing the operator console, a scatter plot, the graph tool, the datalogging screen, the instrument programming wizard, a 3-D graph tool, a histogram, a calibration plot, a 3-D analog shmoo plot, and Geotest's DIOEasy vector editor.

As we have illustrated with our two examples, PXI instrumentation offers the capabilities and test throughput to address a range of semiconductor test applications. The introduction of PXI Express with a bus bandwidth greater than 4.5 Gbytes/s offers even higher performance. In addition, the PXImc (PXI MultiComputing) standard (Refs. 4 and 5) supports the connection of two or more high-performance intelligent subsystems using PCI or PCI Express interfaces, further

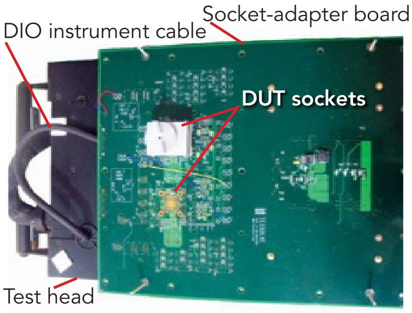

FIGURE 3. This socket-adapter board for a digital transceiver can accommodate dual-site testing.

Table 1: Incumbent vs. PXI-based test-system characteristics for a digital-isolation device

Parameter	Incumbent tester	PXI-based tester
Load-board complexity	Special circuit for high voltage	No special circuitry
External instrumentation	High-voltage supply	None; high-voltage plug-in card available
Software programming tools	Limited tools available	Range of tools to support different stages; includes the tools supplied by the PXI instrument vendor
Multisite ability	Not proven	Can be done
Tester footprint	>20 ft^2	<6 ft^2
Tester weight	>1000 lb	<100 lb
Power requirements	>2 kW	600 W
Cost of tester	>$400,000	$120,000

Table 2: Customer specifications for digital-isolation device tester

Customer specifications	PXI-based system features
560-V to 2500-V DC signal, preferably without any external power supplies for transformer isolation and functional testing	12-bit PXI ADC board and DAC board interfaced with a custom-bus-based proprietary intelligent signal-conditioning 0-V to 2500-V high-voltage VI board.
Multiple power supplies up to 5 V, 5 A	12-bit PXI ADC board plus DAC board interfaced with custom-bus-based proprietary intelligent signal-conditioning VI board
16 digital channels with vector patterns; drive and strobe capability supporting data rates of more than 20 MHz with deep vector memory for functional testing	Geotest GX5295 32-channel DIO and PMU card with 256 Mbytes of onboard vector memory
12-bit or better PMU for DC and parametric testing	
Very low leakage current measurement in picoamps	PXI 7.5-digit digital multimeter with signal-amplifier board
8-bit or better high-speed digitizing capability with deep onboard memory for skew and switching characteristics testing	PXI 2-Gsamples/s high-speed digitizer
Arbitrary function generation, 8-bit resolution or better	PXI arbitrary function generator with 8-bit, 512-Mbyte memory

Table 3: Incumbent vs. PXI-based test-system characteristics for digital receiver

Parameter	Incumbent tester	PXI-based tester
Stability	Stable, characterization and production testing ready	Stable, characterization and production testing ready
Test cost per second	High	Very low
Tester cost	>$1 million	<$300,000
Upgrading cost for multisite test	Very high	Low
Handler interface for production test	Support for various handler interfaces such as TTL; GPIB ready	Support for various handler interfaces such as TTL; GPIB ready
Tester footprint	>70 ft^2	<10 ft^2
Power consumption, energy costs	High, about $700 per month	Low, about $30 per month

Table 4: Software tools used in example testers

Purpose	Tool name	Functionality
Test program	3MTS Maestro instrument-programming wizard	Test program generation, debug, and run
Datalogging	Maestro datalogger tool	Characterization and production datalogging, data mining, histograms, scatter plots, statistics report
Vector editing and display	Geotest DIO Easy	Vector generation, debug, export, import functionalities
Parameter characterization	Maestro Shmoo Tool	Supports analog and digital shmoo-plot generation for parametric sweep tests for one-, two-, or three-axis analysis
Waveform capture and analysis	3MTS Graph Tool	Real-time waveform capture, curve-tracer analysis, and math processing

enhancing the performance of PXI-based systems by supporting peer-to-peer communication within a PXI chassis and enabling system developers to assemble high-performance signal-acquisition and signal-processing subsystems. The PXI standard offers an extended high-performance roadmap for both current and future semiconductor test needs.

Of course, the electronics market will continue to make use of dedicated memory testers and logic ATE systems that meet the cost-of-ownership requirements for specific high-volume products. But as the capabilities and performance of PXI-based test systems continue to grow to address an ever-wider range of device types, the use of PXI-based testers combined with BIST will increasingly offer an economically and technically compelling alternative to traditional "big iron" ATE. T&MW

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ACKNOWLEDGEMENT

For assistance with the digital broadcast receiver example, the authors would like to thank Ganesh Veeramani, semiconductor test lead, and Rajarajan K, semiconductor test engineer, at Tessolve Services in T. Nagar, Chennai, Tamil Nadu, India.

Debugging low-power designs

A logic analyzer and an oscilloscope can help you debug embedded systems designed with energy-management techniques.

BY GINA BONINI, TEKTRONIX

Energy-management techniques, such as dynamic-power management, dynamic voltage scaling, and dynamic frequency scaling, have emerged as effective ways to reduce power consumption—a critical requirement in today's embedded-system designs. These schemes reduce power consumption by shutting down idle components or reducing the performance of components to provide just enough performance for a task. These techniques work on both processing elements, such as CPUs, FPGAs, and ASICs, and the communication buses that transfer data between these elements. But unfortunately, these techniques also increase the complexity of test for design validation and debug.

Power dissipation

Static-power dissipation occurs when you turn on a processing element, and dynamic-power dissipation occurs during computations. You can represent the total power dissipation as the sum of the static power and the dynamic power.

The static-power dissipation occurs even when no computations are occurring. Leakage power and bias power are the main contributors to static-power usage.

Dynamic-power dissipation results from short-circuit power and switching power. The short-circuit power consumption is proportional to the supply voltage. The switching power dissipates when the parasitic capacitors of the transistor gates charge and discharge during computational tasks.

So, the processing element's power usage is equal to the sum of leakage power, bias power, short-circuit power, and switching power, where leakage power and bias power contribute to static power, and short-circuit and switching power contribute to dynamic power.

The switching power is the dominant source of power usage, accounting for approximately 90% of the total power that mainstream processing elements consume (Ref. 1). The common equation for calculating the switching power of a processing element is:

$$P_{SW} = \alpha \times C_L \times V_{DD}^2 \times F$$

where P_{SW} is the switching power; α is a constant representing the switching activity for the computational task; C_L is the effective circuit-load capacitance, which you can assume to be a constant determined by the complexity of the

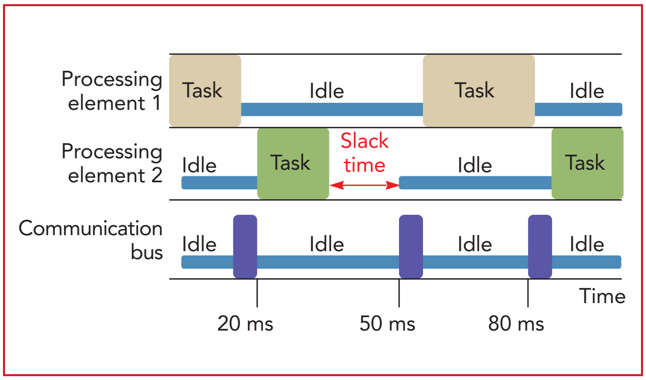
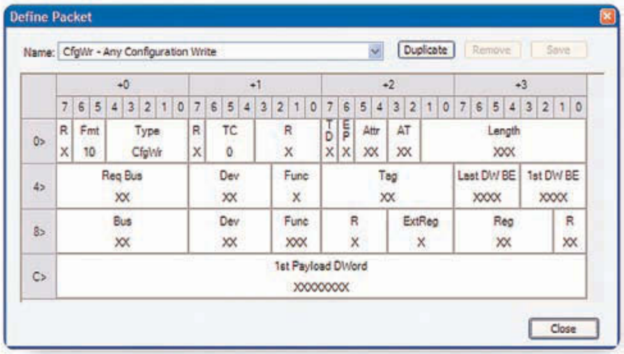


FIGURE 1. In dynamic voltage and frequency scaling, the system's schedule allows for 30 ms for Processing element 2 to complete a task.



Name: CfgWr - Any Configuration Write

	+0								+1								+2								+3							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0>	R X	Fmt 10		Type CfgWr					R X	TC 0			R X				TD X	EP X	Attr XX		AT XX		Length XXX									
4>	Req Bus XX								Dev XX					Func X			Tag XX								Last DW BE XXXX				1st DW BE XXXX			
8>	Bus XX								Dev XX					Func XXX			R X				ExtReg X				Reg XX						R XX	
C>	1st Payload DWord XXXXXXXX																															

FIGURE 2. A logic analyzer with a serial module for PCIe is the troubleshooting tool of choice because it allows you to trigger on a transaction-layer-packet configuration write based on the bus, device, and function number.

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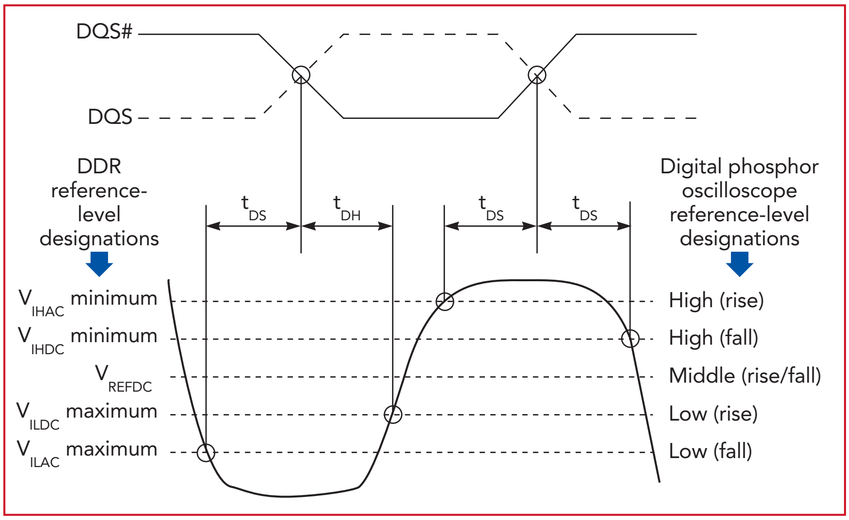


FIGURE 4. Timing measurements on data signals use both the AC and the DC high and low input-voltage levels.

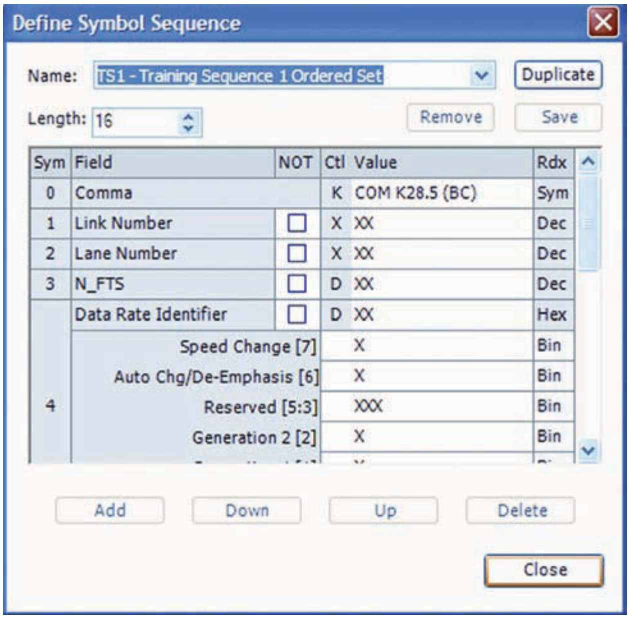
design and the circuit technology; V_{DD} is the supply voltage; and F is the clock frequency (Ref. 2).

The equation above shows that you can reduce either the processing element's frequency of operation or the supply voltage to reduce switching-power dissipation. Because switching power is proportional to the supply voltage squared, you can achieve the largest energy savings by reducing the circuit's supply voltage. In some cases, you can achieve further energy savings by also reducing the operation frequency.

You must carefully apply this technique because it increases processing time. Because power dissipation over time determines energy dissipation, you may achieve no energy savings if extra processing time is necessary. Careful application of both frequency and voltage scaling, however, offers higher energy savings than voltage scaling alone. Reducing supply voltage also reduces leakage-power consumption, improving static-power dissipation (Ref. 3).

Dynamic-power management uses standby or sleep modes to reduce power consumption. Because it takes time and energy to reactivate processing elements and buses, you should carefully apply dynamic-power management to ensure that no violations occur in the system's operation or, in the worst case, no increases in power consumption from reactivation occur. Components still dissipate energy in standby as static power determines.

Dynamic voltage and frequency scaling reduces switching-power dissipation. This process can increase computation time, so you can apply dynamic frequency scaling only when there is slack time in the system-level operation of the design. **Figure 1** shows an example of dynamic voltage and frequency scaling. In this case, the system schedule allows 30 ms for Processing element 2 to complete a task. The processing element completes the task in 15 ms, however, leaving 15 ms of slack time. The supply voltage and operational frequency of this element decrease until the task completes in 30 ms to match the system's schedule. Doing so decreases the power consumption of Processing element 2.



Name: TS1 - Training Sequence 1 Ordered Set

Length: 16

Sym	Field	NOT	Ctl	Value	Rdx
0	Comma		K	COM K28.5 (BC)	Sym
1	Link Number	☐	X	XX	Dec
2	Lane Number	☐	X	XX	Dec
3	N_FTS	☐	D	XX	Dec
4	Data Rate Identifier	☐	D	XX	Hex
	Speed Change [7]			X	Bin
	Auto Chg/De-Emphasis [6]			X	Bin
	Reserved [5:3]			XXX	Bin
	Generation 2 [2]			X	Bin

FIGURE 3. This type of dialogue box helps users set up the condition for triggering on a training sequence.

You can also use dynamic-power management to maximize a design's energy efficiency. Even if you apply dynamic voltage and frequency scaling to all components that are adapting their performance to the requirements of the system schedule and minimizing energy consumption, idle times may still occur. You can then use dynamic-power management to shut down components that are idle for a time for even further energy savings.

Bus energy dissipation

Communication between elements is essential in embedded systems with multiple processing elements. With every data transfer over a communications bus, the line capacitance charges and discharges, drawing current from the I/O pins of the elements. The following equation calculates the power that these currents dissipate:

$$P_{CL} = \beta \times C_{BUS} \times F_{BUS} \times V_{TR}^2$$

where P_{CL} is the power loss that these currents dissipate, $\beta \times C_{BUS}$ represents the switched load capacitance of the bus, F_{BUS} is the operational frequency of the bus, and V_{TR} is the transmission voltage.

You can reduce the transmission voltage in communications buses only to a limit because of noise issues. Noise can more easily corrupt low-voltage communications, causing reliability problems. As with dynamic frequency scaling, you can scale down the operational frequency or data-transfer rate of the bus if the system schedule has slack time for

FIGURE 5. To ease setup tasks, a menu-driven interface guides you through a selection process.

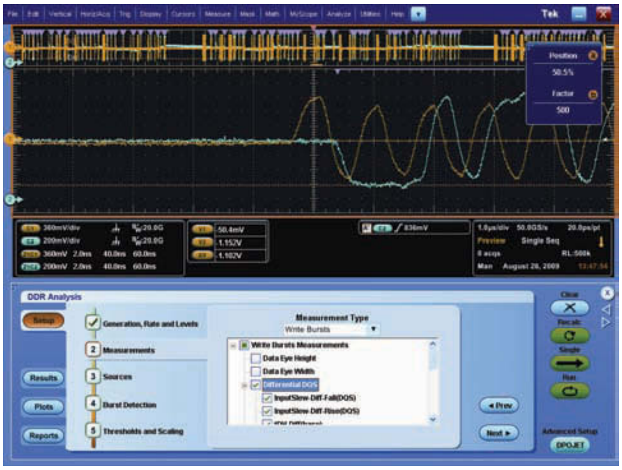
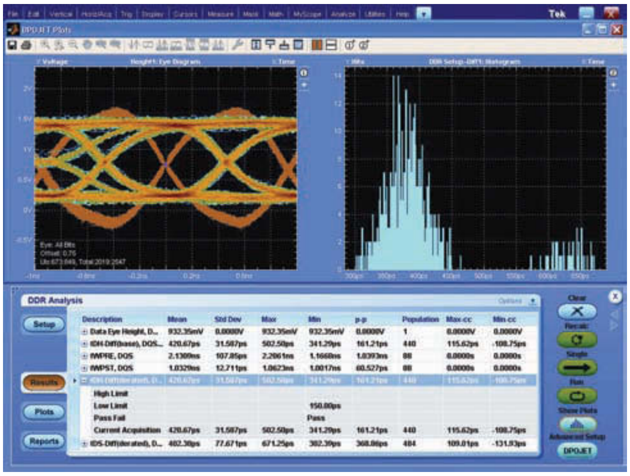


FIGURE 6. The menu groups available measurements according to which signals and probing connections are necessary.



Description	Mean	Std Dev	Max	Min	p-p	Population	Max-cc	Min-cc
Data Eye Height, D...	932.35mV	0.0000V	932.35mV	932.35mV	0.0000V	1	0.0000V	0.0000V
tDH-Diff(base), DQS...	420.67ps	31.587ps	502.50ps	341.29ps	161.21ps	440	115.62ps	-108.75ps
tWPRE, DQS	2.1300ns	107.85ps	2.2061ns	1.1668ns	1.0393ns	88	0.0000s	0.0000s
tWPST, DQS	1.0329ns	12.711ps	1.0623ns	1.0017ns	60.527ps	88	0.0000s	0.0000s
tDH-Diff(derated), D...	420.67ps	31.587ps	502.50ps	341.29ps	161.21ps	440	115.62ps	-108.75ps
High Limit								
Low Limit				150.00ps				
Pass Fail				Pass				
Current Acquisition	420.67ps	31.587ps	502.50ps	341.29ps	161.21ps	440	115.62ps	-108.75ps
tDS-Diff(derated), D...	402.30ps	77.671ps	671.25ps	302.39ps	368.86ps	484	109.01ps	-131.93ps

FIGURE 7. A results panel shows all measurement results with statistical population, spec limits, pass/fail data, and other data.

bus communication. You can also put the bus into a standby state during idle times in an approach similar to dynamic-power management.

Low-power DDR (double-data-rate) DRAM devices and several popular communication buses offer low-power modes. These buses include PCIe (PCI Express), MIPI D-PHY and M-PHY, USB 3.0, and MXM (Mobile PCIe Module). Debugging these buses presents a number of challenges.

Troubleshooting the PCIe low-power mode

PCIe specifications provide active-state power management that conserves power by putting the bus into a power-saving state or dynamically configuring the link's width or speed. Validation and verification of a PCIe bus are complicated because of these features. Problems can arise when the system enters or exits one of the power-saving link states or when the link's width or speed changes dynamically in response to system requirements.

Table 1 lists the PCIe's link power states. To maintain synchronization between the transmitter and the receiver, the bus must transmit idle symbols over the link when there is no data available. The receiver decodes and discards these idle symbols. To save power during these periods, you can put the link into a power-saving state. The power savings and the time to recover back to the L_0 state increase as the link moves from the L_0 state to the L_3 state.

Table 1. PCIe link states

Link state	Description
L_0: active state	All transactions are enabled, and link is operating in normal mode
L_{0S}: low resume latency; energy-saving standby	All power supplies and reference clocks are active, transaction-layer packet and data-link-layer packet transmission are disabled with fast return to L_0 state
L_1: higher latency; low-power standby	All power supplies and reference clocks are active, transaction-layer-packet and data-link-layer packet transmission are disabled
L_2/L_3: staging point for transition to L_2 or L_3	Transaction-layer packet and data-link-layer packet transmission are disabled
L_2: auxiliary powered link, deep energy-saving	Main power supply and reference clocks are off
L_3: link off	Link is in this state when no power is applied

To understand how this situation increases complexity, consider a case in which a PCIe link is in the L_0 state and moves to the L_{0S} state. Immediately after the transition, a transaction-layer-packet configuration write occurs that writes an incorrect value to a register, causing the system to crash. To troubleshoot this problem, you must acquire all the transactions that occur during the transition from the L_{0S} state to the L_0 state.

In such a case, a logic analyzer with a serial module for PCIe would be the troubleshooting tool of choice because it allows you to trigger on an event. For example, in this scenario, the logic analyzer would trigger on a transaction-layer-packet configuration write based on the bus, device, and function number (**Figure 2**).

After you define the trigger, the serial module can bit-lock and align the data across all the lanes of the bus after observing approximately 12 fast-training-sequence packets as the link exits the L_{0S} state and enters the L_0 state. Because the logic analyzer can track the change in the link state, it can acquire all transactions that occur immediately after the bus enters the L_0 state, providing insight into the cause of the system crash.

To save memory, you can also set up the logic analyzer to filter out unwanted data in real time, focusing data acquisition on problem areas. A common use of filtering occurs when the PCIe bus is in the idle state. You can define a filter to filter the idle symbols in real time, storing only the required data and thus making more efficient use of the logic analyzer's memory and capturing more relevant data that helps in troubleshooting the problem.

The PCIe specification also provides for dynamically changing the link's width or speed depending on the need to conserve power or provide performance. These dynamic changes in the link's condition can be challenging to debug.

Consider a case in which the link's width is changing from eight lanes to four lanes. Here, you can use a logic analyzer to trigger on and acquire the training sequences that occur during the link-speed change and the link-width negotiation process, allowing you to validate that the link is training to the correct width. **Figure 3** shows the type of dialogue you use to set up the condition for triggering on a training sequence. In some cases, due to errors in the link, you may not find the required trigger conditions. In such instances, you may need to build a customized sequence and set it as a trigger condition on a lane. This approach is faster than manually looking through the data to figure out the problems in the link. To identify errors in the physical layer, logical analyzers offer link-event triggers. For this trigger, the event could be disparity, an 8/10b error, or an error in framing the data-link-layer or the transaction-layer packets.

Low-power DDR memory

Low-power DDR memory, or mobile DDR, helps reduce energy requirements by providing more efficient device operation. It operates at 1.8 V rather than the more traditional 2.5 V. Low-power DDR DRAM commonly finds use in portable electronic devices, and line-powered electronics are increasingly adopting it as a way to reduce energy requirements.

Reducing operating voltage is a trend that extends beyond low-power DDR memory to more mainstream memory technologies, as well. DDR2, which originally operated at 2.5 V, has seen later variants that lower the requirement to 1.8 V, and further reductions are in development. Similarly, DDR3 once operated at a supply voltage of 1.5 V but will soon see that figure decrease to 1.35 V for some new components. Low-power DDR2, the newest entry in this power-reduction trend, requires only 1.2 V.

You can achieve additional energy savings by reducing the performance of the device. Low-power DDR and other DDR standards specify power-saving modes of operation that reduce performance depending on the system's needs.

Power-saving modes

Because DRAM cells leak off charge, they must regularly refresh their contents during modes of operation requiring maintenance of data. The low-power-DDR-DRAM specification calls for three refresh modes to minimize power dissipation and maintain the required data states. The most basic mode, self-refresh, generates a low-frequency internal clock to maintain the contents of the DRAM. Temperature-compensated self-refresh automatically modifies the internal refresh clock frequency depending on the temperature of the low-power DDR DRAM. During lower operating temperatures, the refresh time can be longer to save power. Partial-array self-refresh maintains data in only a portion of the DRAM.

When the low-power-DDR-DRAM device does not need to retain data and when access to the DRAM is not necessary for several seconds, the device can use the power-down mode.

A system's power consumption is proportional to the frequency at which the clock is changing. The low-power-DDR-memory standard stipulates many power-saving modes that leverage the frequency component of this power equation. The power-saving refresh modes reduce the clock frequency to reduce power consumption. The power-down mode can put the DRAM into standby mode during inactive periods. All of these power-saving modes primarily affect static-power consumption.

You can reduce dynamic-power consumption by optimizing data throughput, allowing the operating frequency of the device to decrease and still meet performance requirements. The ability to do this task is a key differentiator of low-power-DDR-DRAM devices.

Validating DDR DRAM

JEDEC (Joint Electron Device Engineering Committee) has specified the jitter, timing, and electrical-signal-quality tests for validating memory devices. The JEDEC specifications describe a comprehensive set of tests for each memory technology, including parameters such as clock jitter, setup-and-hold timing, signal overshoot, undershoot, and transition voltages. These specified tests are not only numerous but also complex to measure using general-purpose tools.

An example is measurement reference levels. JEDEC specifies certain voltage reference levels that you must use when making timing measurements. **Figure 4** shows the AC and DC high and low input-voltage levels that timing measurements on data signals use. JEDEC defines the levels for rising and falling edges differently. Because of the complexity inherent in the JEDEC-specified measurement methods, including reference levels and pass/fail limits, the preferred approach is to use an application-specific measurement utility for DDR test. Using such a utility ensures that you configure measurements according to the specification, and it also reduces setup time.

With real-time-performance oscilloscopes, DDR software utilities provide a broad set of measurements that conform to the JEDEC specifications. In addition, these utilities allow you to customize many settings to accommodate measurement tasks on nonstandard devices or system implementations and to aid in debugging. To ease setup tasks, a menu-driven interface guides the user through a selection process (**Figure 5**).

The first step of such an interface is to select the DDR generation you want to test and the speed grade of the memory. In addition to the default choices, the use of custom speed settings makes the software adaptable to future technology advances, overclocking applications, and the like. Once you have selected the generation and data rate, the software configures the correct voltage references for measurements.

The next step is to select which measurements to perform (**Figure 6**). The menu groups available measurements according to which signals and probing connections are necessary. The remaining steps guide you on how to probe the needed signals and offer additional opportunities for customizing or adjusting parameters, such as measurement reference levels.

Once the setup is complete, the oscilloscope acquires the signals of interest, identifies and marks data bursts if needed, and makes the selected measurements. A results panel shows all measurement results with statistical population, spec limits, pass/fail results, and other data (**Figure 7**). You can at this point print a report, with an option to also save the waveform data that you used to make the measurements.

Because the captured waveform data is available with the measurement results, you can use this information for further analysis. For example, if a measurement fails the spec limits, you can identify exactly where in the waveform record the failure occurred and then zoom in on the region of interest to investigate the exact signal details and characteristics at the time of failure.

System-level energy-management techniques look at the system-level operation of a design for opportunities to lower power consumption by shutting down components or scaling voltage and frequency. Test-and-measurement tools have evolved to help designers debug systems in the face of this increased complexity. For instance, logic analyzers offer trigger capability with a layout similar to the definitions in the standard they are testing—a helpful technique in finding elusive problems resulting from active-state management.

Similarly, validating DDR-DRAM devices requires performing the numerous tests in the JEDEC specifications, a time-consuming and complicated task. By using specialized software together with a high-performance real-time oscilloscope, you can access a broad set of automated measurements, simplifying the validation of memory devices. T&MW

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A version of this article first appeared in the October 21, 2010, issue of EDN.

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Keithley upgrades RF vector signal analyzer, introduces upconverter

Keithley Instruments at the International Microwave Symposium announced that it has upgraded its RF vector signal analyzer line with new capabilities that reduce signal-acquisition and measurement times. Keithley also highlighted its new Model 2891-IQ upconverter. More

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Microscan miniature imager reads direct part marks

The Mini Hawk from Microscan packs DPM reading algorithms into a miniature imager for use in barcode and 2-D track, trace, and control applications.

Elma upgrades rack-mount desktop enclosure

Elma Electronic has upgraded its Type 15 StyleBox enclosure with several key features, including more color choices and a new handle assembly.

Tektronix scope software debugs DDR3 memory designs

Tektronix announced the third-generation of its DDR analysis software for the

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SMUs give multiple views

Agilent Technologies has entered the benchtop SMU (source-measure unit) market with the introduction of the B2900A series. Consisting of four models, the B2900A series can produce four-quadrant power up to ±210 VDC, ±3 A continuous or ±10.5 A pulsed. The series has 2 one-channel models (B2901A and B2911A) and 2 two-channel models (B2902A and B2912A). The one-channel instruments have source resolution of 1 pA and 1 µV and sample at 50 ksamples/s, while the two-channel units have 10-fA and 100-nV resolution and can sample at 100 ksamples/s. All models have 6.5-digit measurement resolution.

The user interface lets you view voltage and current as either single measurements with a digital readout or as graphs. When operating in graph view, the SMUs can display I-V curves for a device under test, much like a curve tracer. The two-channel models give these displays for both channels; in addition, they have a rolling display, which operates like a chart recorder.

You can operate the SMUs from the front panel through a numeric keypad and soft keys located under and alongside the display. These keys let you set voltage and current levels, sweep speeds, pulse widths, and triggers. A front-panel USB port lets you store setups and data. Front- and rear-panel jacks give access to inputs and outputs from both ends of the unit.

The B2900A series SMUs also have 14 open-drain digital I/O ports on the rear panel for controlling external devices such as alarms. When operating as digital inputs, the lines can become hardware triggers. For remote automated control, the SMUs have USB, LAN, and GPIB ports. Agilent also provides software that can control up to four SMUs. When using the LAN interface, you can control the instruments through a browser because they have built-in Web servers.

Prices: B2901A—$5671; B2902A— $8248; B2911A—$8042; B2912A—$12,451. *Agilent Technologies, www.agilent.com/find/B2900A.*

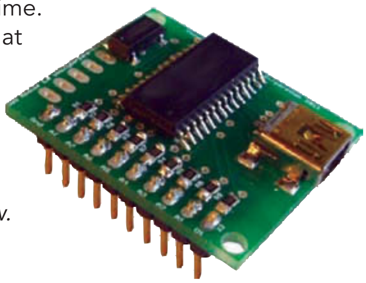
Module counts analog and digital signals

When you need to embed some analog inputs and a digital input into a system, CyberData's USB-TACH-02 tachometer/event counter/frequency counter just might fit the bill. Packaged on a 10-pin board, the module has seven analog inputs and one digital input.

The analog channels, which share a common 24-bit counter, can capture signals with levels as low as 100 mV with gain from 1 to 48. Input frequency is DC to 100 kHz.. An analog-tracking channel lets you monitor a selected analog channel after the programmable amplifier boosts the signal to a level compatible with the trigger level. You can use the analog channels as digital channels by setting a threshold voltage of 1.65 V, 2.06 V, 2.48 V, or 2.89 V.

The digital-only channel has a 4-MHz maximum frequency with a fixed threshold level of 1.65 V. The digital channel has a dedicated 24-bit internal counter, which the host computer can read at any time.

The module has a USB port that lets it communicate with a computer. Drivers are available for Windows CE, and Windows 98 through Windows 7, plus MacOS and Linux.



Price $97.50. *CyberData, www.CyberData-Robotics.com.*

Anritsu expands DMR test capabilities

Anritsu has introduced two options that allow its LMR Master S412E to conduct digital-modulation analysis and generation and coverage mapping based on the ETSI DMR (Digital Mobile Radio) Tier 2 protocol. The first option—the modulation-analysis option—enables the LMR Master S412E to make measurements on the transmission characteristics of DMR networks. The instrument can test emerging narrowband as well as broadband digital public-safety systems. With the second option, the analyzer

can also generate DMR signals. The analyzer is also capable of generating data-modulated signals in other formats, including P25 and NXDN.

To perform DMR coverage measurements, the user connects a receive antenna and a GPS antenna to the handheld analyzer. The instrument automatically stores results, along with the GPS location. Traces of mapping data are automatically saved and can be later recalled and viewed from the front panel of the LMR Master S412E. The battery-powered instrument can provide cable and transmission at –115-dBm signal levels. A standard transmissive color display is viewable in direct sunlight and at wide viewing angles.

Base prices: DMR options—$1875. LMR Master S412E—$13,950. *Anritsu, www.anritsu.com.*

VNAs add dynamic range, cut measurement times

Designed for demanding applications in the production and development of RF components, the R&S ZNB and R&S ZNC vector network analyzers from Rohde & Schwarz feature a dynamic range up to 140 dB and a sweep time as low as 4 ms for 401 points. The network analyzers cover frequency ranges from 9 kHz to 3 GHz, 4.5 GHz, or 8.5 GHz. Both instruments have a 12.1-in. diagonal touch screen that allows users to access all instrument functions with no more than three operating steps.

The R&S ZNB covers the frequency range from 9 kHz to 4.5 GHz or 8.5 GHz and is available both in two-port and four-port models. It features a dynamic range of 140 dB, trace noise of 0.004 dB (RMS), and output power of up to +13 dBm, which can be adjusted electronically over a 90-dB range. The company says the instrument is suited for making measurements on high-blocking filters or amplifiers that must be manually adjusted on high-volume production lines.

The R&S ZNC, with a frequency range from 9 kHz to 3 GHz, is available with two test ports and offers a sweep time of 11 ms with 401 points and a dynamic range of up to 130 dB. Its primary use is for testing passive RF components, such as filters or cables.

Rohde & Schwarz, www.rohde-schwarz.com.

40-GHz socket handles 23x23-mm BGAs

Using Ironwood Electronics' SM-BGA-9000, you can socket 23x23-mm, 0.8-mm-pitch BGA packages from STMicroelectronics on any application board, while achieving performance equivalent to a direct-solder version. The manufacturer also claims that the socket is made of an elastomer suitable for applications requiring high speed, low inductance, high endurance, and a wide temperature range.

The SM-BGA-9000 operates at bandwidths of up to 40 GHz with less than 1 dB of insertion loss. It dissipates 4.5 W with a heat-sink compression screw and can be customized to dissipate up to 100 W. Contact resistance is typically 15 mΩ per pin. Other specifications include an operating temperature range of –55°C to +150°C, pin self-inductance of 0.10 nH, mutual inductance of 0.007 nH, and a current capacity of 4 A/pin.

Mounted onto the target printed-circuit board without soldering, the SM-BGA-9000 occupies a small footprint, extending just 2.5 mm on each side of the targeted device. It is constructed with a shoulder screw and swivel lid that allows quick insertion of ICs.

Price: $1311 each. *Ironwood Electronics, www.ironwoodelectronics.com.*

JEOL launches stage-navigation system

A point-and-shoot navigation system from JEOL USA makes finding precise locations on a sample faster and easier for users of SEM (scanning electron microscope) and EPMA (electron probe x-ray microanalyzer) systems. The SNS (Stage Navigation System) combines software with an externally mounted CMOS color camera that functions as a low-magnification optical microscope and eliminates the need for a dedicated port on the electron column.

Users simply record an image of the sample, send the image to the SEM, place the sample on the sample stage, and click on the recorded image to specify the area of interest. The software automatically positions the stage with pixel precision to the exact area of the sample to be examined.

SNS software is optional with newer JEOL tungsten, LaB6, or field-emission SEMs and EPMAs. It can be used with either a CCD camera or with the stand-alone SNS camera. The externally mounted 3-Mpixel SNS camera is secured on a camera base and can be located anywhere in the lab. A docking stand simulates the JSM-6XX0 series SEM and the FEG series stage.

The SNS camera offers selectable fields of view and uses a high-frequency variable light source. An optional transmitted polarized illuminator is also available.

JEOL USA, www.jeolusa.com.

Ixia's 10GE load module scales to 384 ports

Aimed at high-density switch-fabric testing, the Xdensity 10GE load module from Ixia packs 32 ports on a single-slot module, scaling up to 384 ports in a single XM12 chassis to deliver 3.84 Tbits of test traffic. The high port count per module reduces both the total power consumption and total footprint of a large test bed.

Together with Ixia's IxNetwork test software, the Xdensity load module reduces the complexity of large-scale testing by providing high-scale Layer 2–3 traffic generation, straightforward large-port test-configuration setup, and highly integrated automation. Ixia says Xdensity helps network equipment manufacturers validate a full range of traffic throughput, latency, and networking scenarios for data-center switch fabrics.

Xdensity performs hardware-based, wire-speed latency measurements and requires no other cards to be in the test bed. Advanced measurements include four latency modes, sequence checking, misdirected packets, packet loss duration, and receive rates. Dynamic traffic support gives you the ability to change the rate and frame size on the fly without stopping and restarting.

Ixia, www.ixiacom.com.

Teseq adds USB interface to RF amplifiers

An integrated USB port is now available on Teseq's CBA series Class-A broadband power amplifiers. Intended for EMC immunity-test applications, the CBA series covers frequency ranges of 10 kHz to 6 GHz and power levels from 12 W to 1000 W.

When fitted with the USB port, the amplifiers can be switched remotely from standby to operational mode. They can also be controlled with Teseq's Compliance 5 test software, which lets you monitor status, local lockout, interlock, and fault conditions. The interface comes with a dynamic link library file that enables control of the unit using other test software packages, as well as a simple program that provides direct control of the amplifier via a PC.

Teseq, www.teseq.com.

Test adapters certify Cat 5e, 6, and 6a cables

Plugged into Fluke Networks' DTX cable analyzer, the company's new patchcord test adapters certify both shielded and unshielded Category 5e, 6, and 6a cable assemblies to ANSI/TIA 568-C and ISO 11801:2010 standards. The DTX handheld cable analyzer and its companion adapters offer an automated test method for ensuring that patchcords and equipment cords meet test requirements. With this setup, you can measure all key patchcord test parameters, including wire map, length, propagation delay, delay skew, near-end crosstalk, resistance, and return loss.

Fluke Networks, www.flukenetworks.com.

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VOL. 31, NO. 6

Subscription Policy: Test & Measurement World® (ISSN 0744-1657) is published monthly except January by UBM Electronics, 600 Community Dr., Manhasset, NY 11030-3825. Periodicals postage paid at Manhasset, NY, and additional mailing offices. SUBSCRIPTIONS: Free to qualified subscribers as defined on the subscription card. Rates for nonqualified subscriptions, including all issues: 1 yr. $150, 2 yrs. $250, 3 yrs. $300. Except for special issues where price changes are indicated, single copies are available for $10 (US orders) and $15 (foreign orders). Buyer's Guide issue is available for $35 (US orders) and $40 (foreign orders). For telephone inquiries regarding subscriptions, call 763-746-2792. E-mail: tmw@omeda.com. CHANGE OF ADDRESS: Notices should be sent promptly to P.O. Box 47461, Plymouth, MN 55447. Please provide old mailing labels as well as new address. Allow two months for change. NOTICE: Every precaution is taken to ensure accuracy of content; however, the publishers cannot accept responsibility for the correctness of the information supplied or advertised or for any opinion expressed herein. **POSTMASTER: Send address changes to Test & Measurement World, P.O. Box 47461, Plymouth, MN 55447. Canada Post: Publications Mail Agreement 40612608. Return undeliverable Canadian addresses to: BleuChip International, P.O. Box 25542, London, ON N6C 6B2.**

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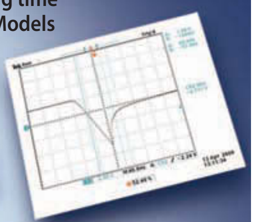
BPA WORLDWIDE

AVR-CD1-B Test System



Typical Output Waveform 2 A/div, 40 ns/div

ADVERTISER INDEX

JIM MAGINN
President/CEO
AR RF/Microwave
Instrumentation
Souderton, PA

In 2009, Jim Maginn was named president of AR RF/Microwave Instrumentation, having previously served as senior VP/CEO since 2006. Maginn joined AR in 1992 as engineering manager, having held defense-related engineering management posts with several leading firms. He was promoted to VP of engineering and manufacturing in 1994 and to senior VP and COO in 1998. Maginn's career began in 1975 with the Department of Defense, where he was a radar systems engineer on the US Army Firefinder Radar development program and later at the Naval Air Development Center. He holds a BSEE from Villanova University and a master's in industrial engineering from Texas A&M.

Contributing editor Larry Maloney conducted a phone interview with Jim Maginn about the changing requirements for EMC test.

New weapons for the EMC arsenal

Q: Over the last decade, how have EMC (electromagnetic compatibility) demands changed for test engineers?
A: More test engineers see the need for higher field strengths and higher frequencies—even up to 60 GHz. Test requirements also have become more stringent as a result of tougher global standards on EMC. Whether it's a car or an airplane, we see a greater mix of instruments and frequencies that can generate interferences. In higher-frequency testing, we also see more demand for accuracy and linearity in test signals—and less harmonics.

Q: Which applications currently account for the greatest share of your company's EMC test business?
A: Military test has become more important, taking over from automotive, industrial, scientific, and medical, which once dominated our business. For example, AR recently delivered a 16-kW solid-state power amplifier to BAE Systems in the UK for its facility for EMC testing. This Model 16000A225 amplifier covers frequencies in the range of 10 kHz to 225 MHz and targets applications that require instantaneous bandwidth, high gain, and very high power.

Q: What kinds of applications are driving such high-performance EMC test?
A: Today, you are seeing many more instances of companies doing EMC tests on entire vehicles, such as cars and airplanes, rather than testing components or subsystems on a piecemeal basis. This need for both higher power and higher frequency has led us to redesign our A series and S series of microwave amplifiers to go up to 18 GHz, with the S series going up to over 1250 W in power. These are astronomical increases compared to the capabilities of these devices just a few years ago.

Q: What types of products are typically combined in an EMC test suite?
A: The centerpiece is a set of amplifiers suitable to whatever frequencies that need to be tested. The test engineer can also choose from an array of antennas, couplers, power meters, and field probes, such as our new laser-powered E-field probes, one of which covers the 2-MHz to 40-GHz range, while the other covers the entire 2-MHz to 60-GHz range. Finally, there's the software needed to control the tests. Increasingly, engineers are asking us to provide turnkey test solutions that incorporate all these test components, plus an anechoic chamber, rather than having to pull together all the elements themselves. This trend runs across all our markets, particularly when engineers need to test an entire end product.

Q: What improvements are you making in software for EMC applications?
A: The whole idea is to make it as easy as possible to perform tests. The newest version of our test software, SW1007, lets users select built-in test procedures and provides formatted reporting capabilities. An updated user interface includes a new tab system that makes selecting the predefined test standard much easier. Users can also create and easily edit parameters to conduct custom tests. Each module in this new software is based on a different type of EMC testing, and an Equipment Manager tool enables users to enter equipment one time, and then access that equipment from any of the software's modules.

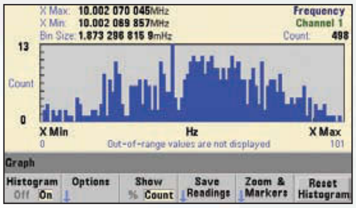
In the past, our software primarily governed tests having to do with radiated conducted susceptibility, but now we can also test for conducted and radiated emissions. We also integrate this software with our new digital-processing-based EMI (electromagnetic interference) receiver for emissions testing. So, we now cover both sides of the street: immunity and emissions. T&MW

Jim Maginn answers more questions about new EMC technologies in the online version of this interview: www.tmworld.com/2011_07.

To read past "Viewpoint" columns, go to www.tmworld.com/viewpoint.

"I never expected a frequency counter to do so much, so fast."

Speed, resolution and accuracy are just the beginning.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X Min: 10.002 069 857MHz
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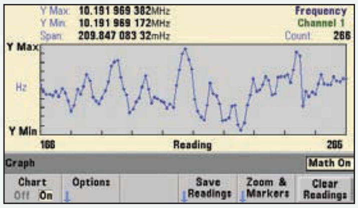
Count: 498


Y Max: 10.191 969 382MHz
Y Min: 10.191 969 172MHz
Span: 209.847 083 32mHz
Count: 266

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53220A	350 MHz, 12 digit/s, 100 ps, Universal Frequency Counter / Timer
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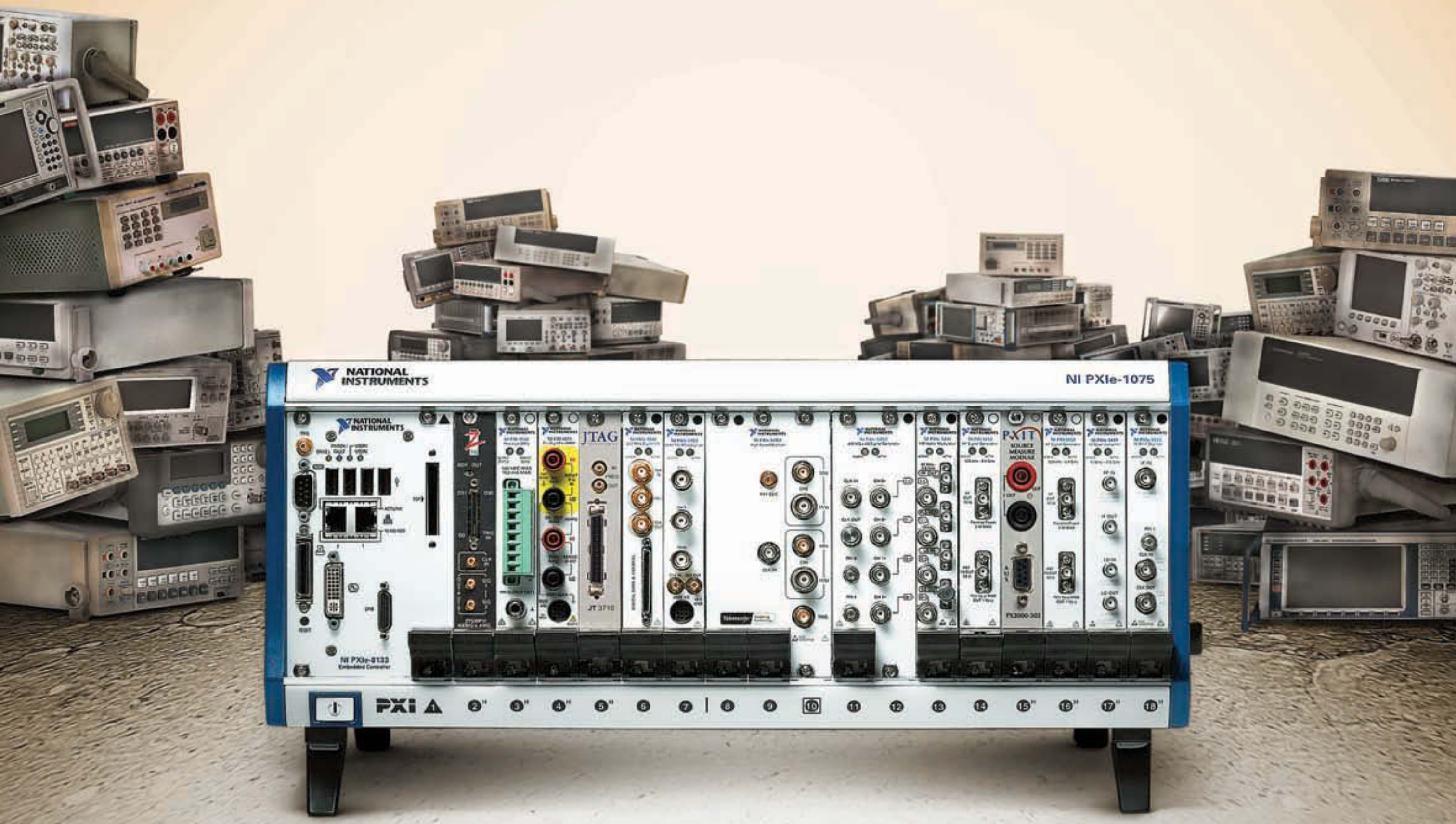

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